

COMPAL CONFIDENTIAL

BROADMOOR MLK 14 UMA(TBT)

ALDER LAKE-P
2021-01-18

REV : 1.0 (A00)

MODEL NAME : HDB45

PCB NO : LA-L871P

BOM P/N :

GPIO MAP : X13_ADL_P GPIO map Rev0.4_20210329

PWR Circuit: X13 BROADMOOR MLK 14_UMA_ADL_P_DDR5_PWR20220110A

@ : Nopop Component
EMI@ : EMI Component
@EMI@ : EMI Nopop Component
ESD@ : ESDComponent
@ESD@ : ESD Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
CONN@ : Connector Component
@CONN@ : Nopop Connector Component
MIPI60@ :MIPI Component
NMIPI60@ :Non MIPI Pop Component
VPRO@ : vPro Component
NVPRO@ : Non-vPro Component
WWAN@ : WWAN Component
WWANRF@ : WWAN RF Component
CCD@ : CCD function
TGSSD@ : Teton Glacier Component

ST@ : ST TPM Component
NU@ : Nuvoton TPM Component
CPU@ : CPU
5200B@ : MEC5200 ver.B Chip
5200C@ : MEC5200 ver.C Chip
TD4@ : Pop TD4.1.1 Switch
NTD4@ : Depop TD4.1.1 Switch
JUMP@ : Jump solder and short
@JUMP@ : Jump no solder
ACCST16@ : Acc sensor Stmicron 16-bit
BB@ : TBT Intel retimer Burnside Bridge
PS8830@ : TBT Parade 3rd party Retimer
DUDC@ : DUDC Component
NDUDC@ : Nopop DUDC Component
SD@ : SD support Component
NSD@ : non SD support Component
DDREN_EC@ : DDR5 VR enable from EC
DDREN_SUS@:DDR5 VR enable from PCH

MB PCB

Part Number	Description
DA23JS00101	PCB HDB45 LA-L871P LS-R491P UMATMAC A31

Layout Dell logo



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REV:A00
PWB:

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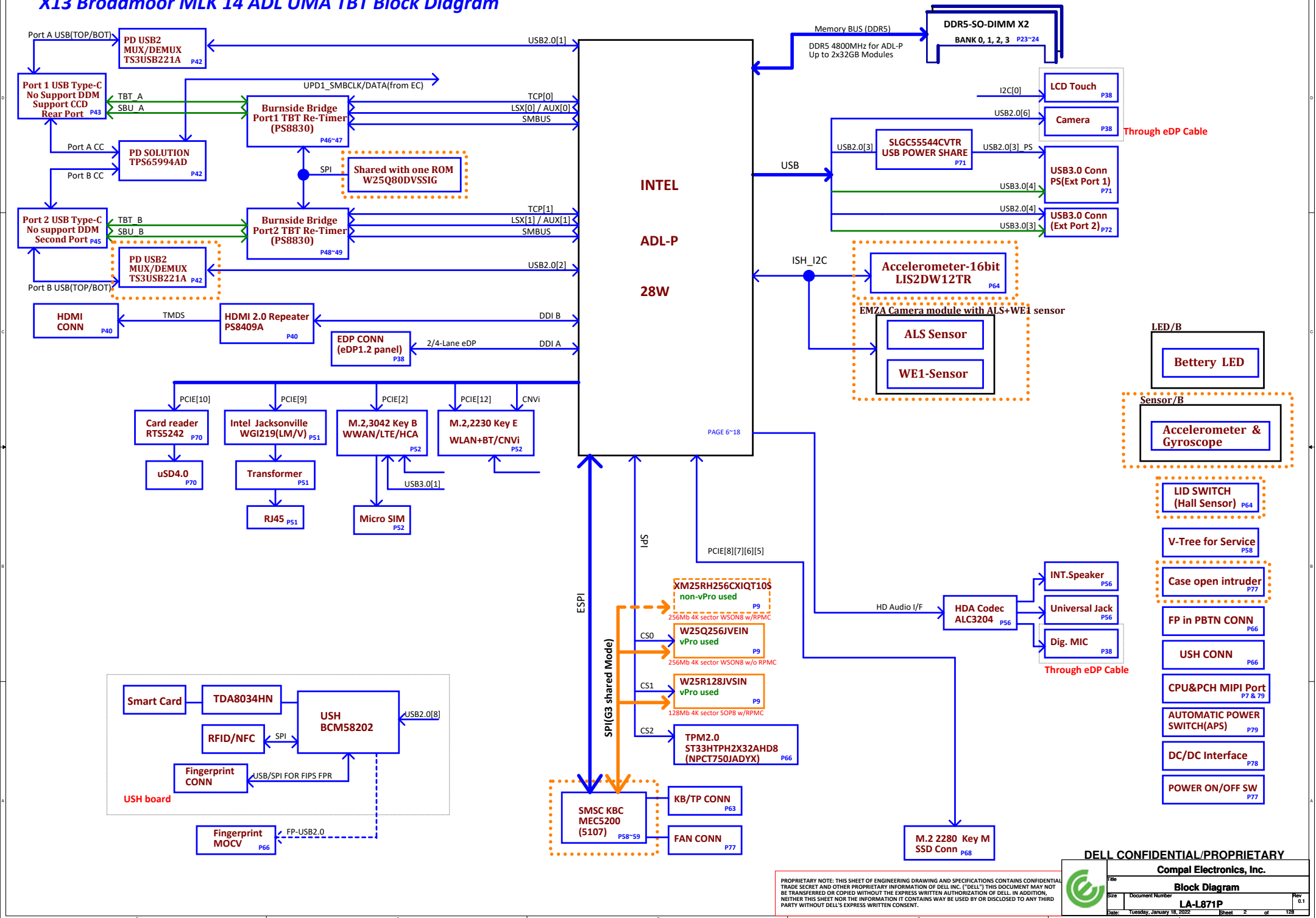
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Cover Sheet

LA-L871P

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X13 Broadmoor MLK 14 ADL UMA TBT Block Diagram



Refer to PDG "power stste" section

Rails	Rail in SPMLK	S0/M0	C10	S0ix/Moff	S3/M3	S3/Moff	S4 and S5/M3	S4 and S5/Moff	G3
VCCRTC	+3.3V_VCCRTC	ON	ON	ON	ON	ON	ON	ON	ON
VCCDSW_3P3	(+3.3V_PRIM) +3.3V_ALW_DSW	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA(VDC)	+17.8V	ON	ON	ON	ON	ON	ON	ON	No Power
VCCPRIM_3P3	+3.3V_PRIM	ON	ON	ON	ON	ON	ON	ON	No Power
VCCPRIM_1P8	+1.8V_PRIM	ON	ON	ON	ON	ON	ON	ON	No Power
V3.3M	subsystem 3.3V	ON	ON	OFF	ON	OFF	ON	OFF	No Power
V1.8M	subsystem 1.8V	ON	ON	OFF	ON	OFF	ON	OFF	No Power
VDD2	+1.1V_MEM	ON	ON	ON	ON	ON	OFF	OFF	No Power
VPP	NA	ON	ON	ON	ON	ON	OFF	OFF	No Power
VCC1P05_PROC	+1.05V_PROC	ON	ON	ON	ON	ON	ON	ON	No Power
VCCIN_AUX	+VCCIN_AUX	ON	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	No Power
VCC1P8_PROC	not use	ON	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	No Power
VCC_MIPILP	not use	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCCORE	+VCCIN	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCGT	+VCC_GT	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power

Figure 1. Flexible HSIO Lane Multiplexing in PCH-P

PCH-P	Flex HSIO Lanes											
	0	1	2	3	4	5	6	7	8	9	10	11
HSIO Type and Lane	USB 3.2 Gen 1x1/2x1 #1	USB 3.2 Gen 1x1/2x1 #2	USB 3.2 Gen 1x1/2x1 #3	USB 3.2 Gen 1x1/2x1 #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	GbE	UFS 1x2	PCIe* #12
												SATA 1
				PCIe* #4							SATA 0	
			PCIe* #3					GbE			Lane 1	
		PCIe* #2								Lane 0		

PCH HSIO Port	USB3	GbE	PCIE	SATA	DEVICE
USB3-1			PCIE-1		M.2 3042(LTE)
USB3-2			PCIE-2		M.2 3042(WWAN)
USB3-3			PCIE-3		Type-A Port2
USB3-4			PCIE-4		Type-A Port1
			PCIE-5		NA
			PCIE-6		
			PCIE-7		
			PCIE-8		
	V		PCIE-9		LOM
			PCIE-10		CARD READER
			PCIE-11	SATA 0	NA
			PCIE-12	SATA 1	M.2 2230(WLAN)

PCH USB2.0	DEVICE
1	Type-C Port1
2	Type-C Port2
3	Type-A Port1
4	Type-A Port2
5	NA
6	UF Camera
7	M.2 3042(WWAN)
8	CV3
9	FPR in PB
10	M.2 2230(BT)

CPU HS PORT	DEVICE
DDI-A	LCD
DDI-B	HDMI2.0
TCP0	Type-C Port1
TCP2	NA
TCP3	NA
PCIE4A[0-3]	M.2 2280 (SSD)
PCIE4B[0-3]	NA
PCIE8[0-7]	NA

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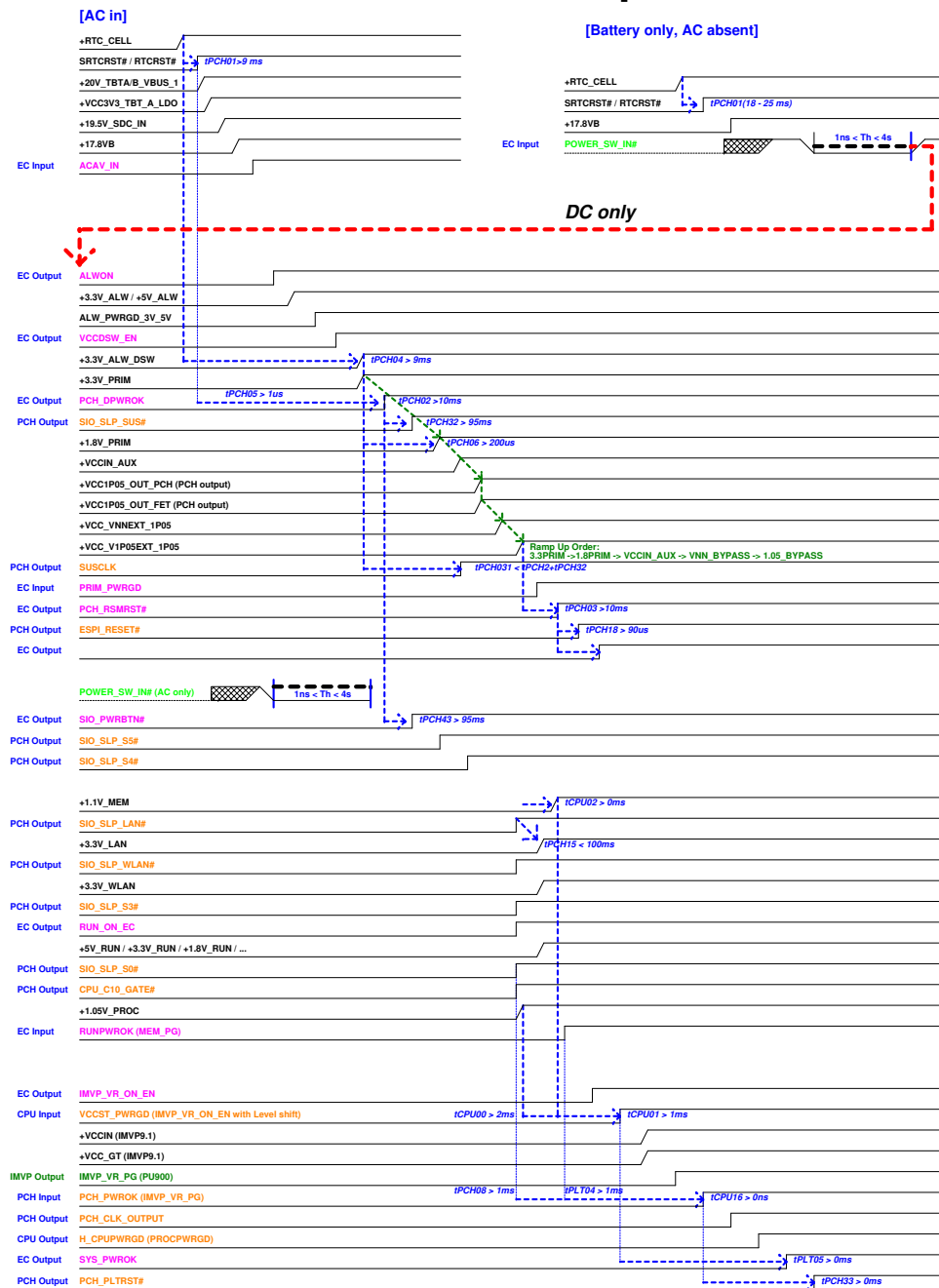
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Port assignment			
Title	LA-L871P		
Size	Document Number	Rev 0.1	
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Power Sequence

G3 -> S0 Non deep



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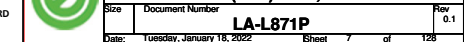
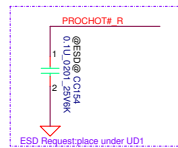
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Power Sequence

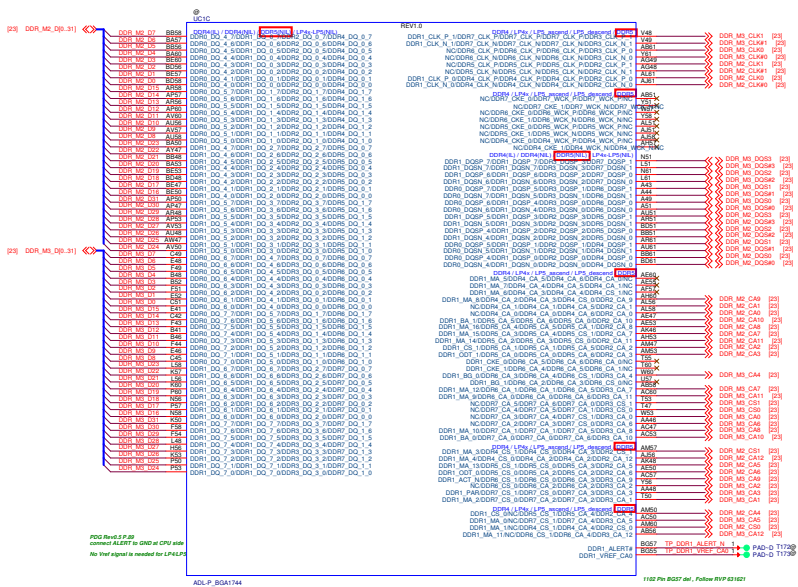
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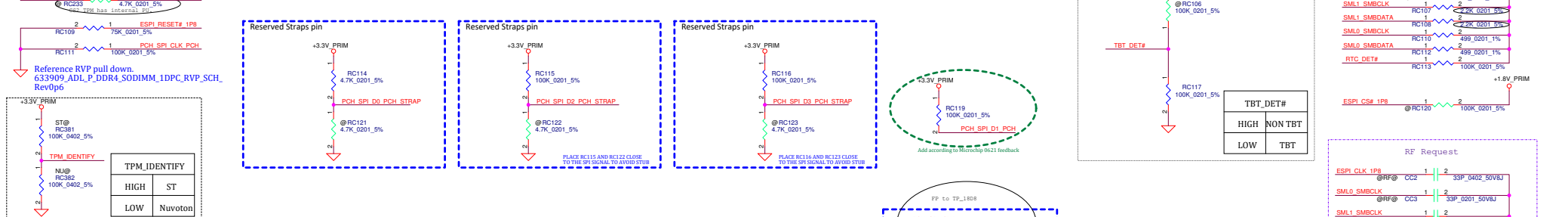
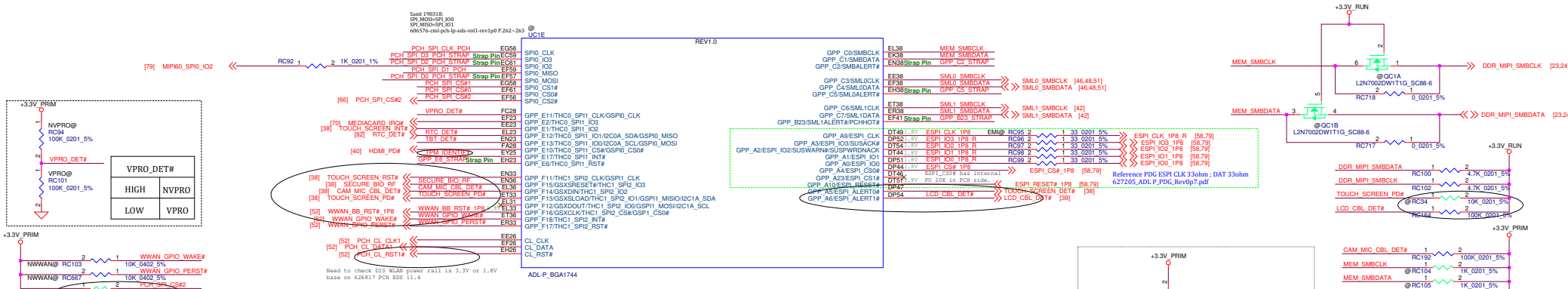
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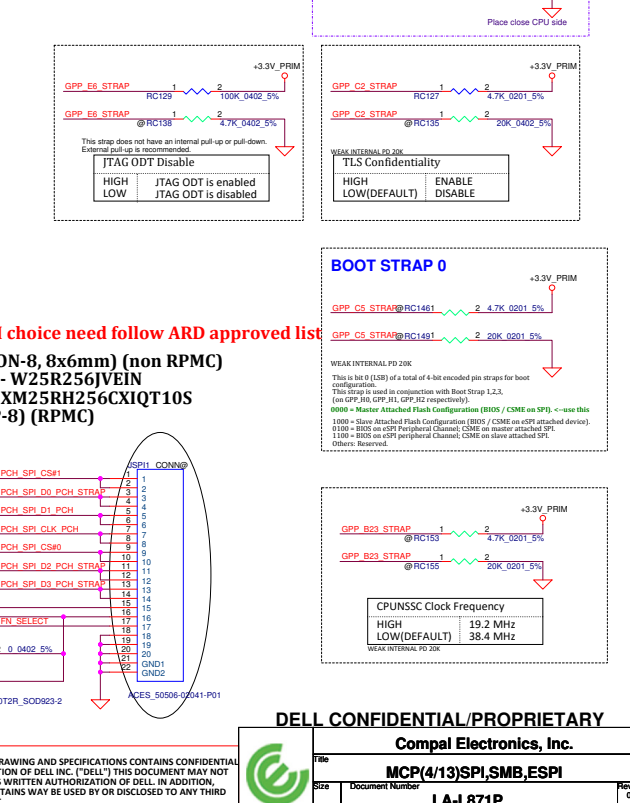
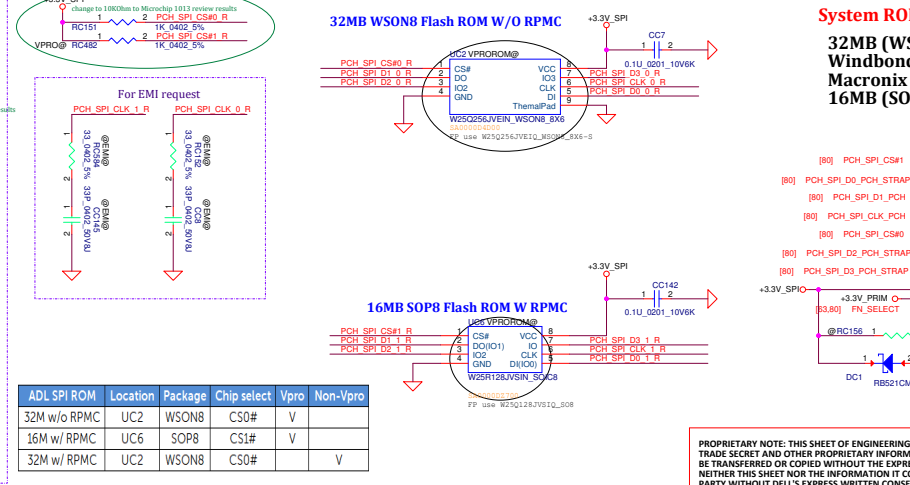
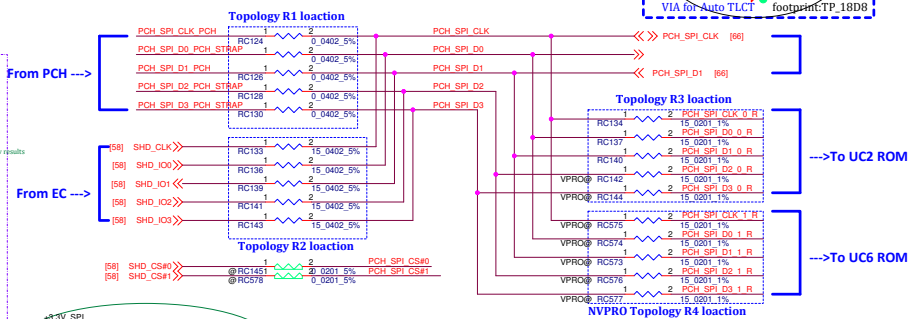
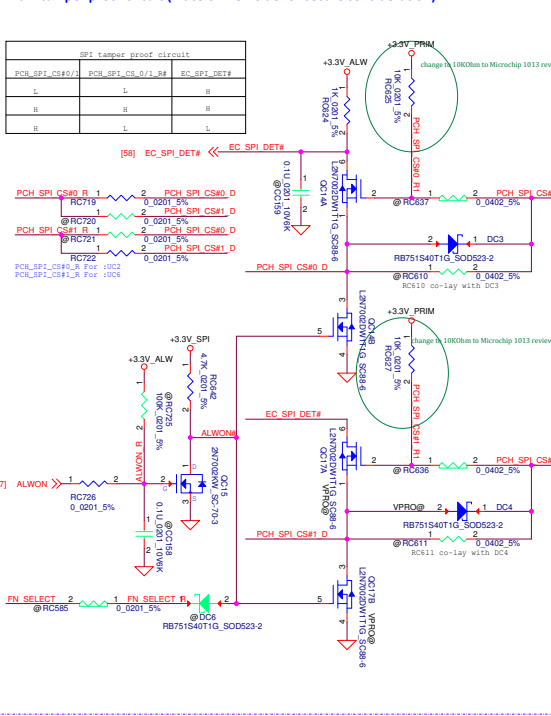
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**EC G3 SPI Flash Sharing with Wire-OR(2 Flash and 1TPM)
Reference627205_ADL P_PDG_Rev0p81.pdf
at P.474**

SPI tamper proof circuit (Place on TOP side for secure consideration)



ADL SPI ROM	Location	Package	Chip select	Vpro	Non-Vpro
32M w/o RPMC	UC2	WSON8	CS0#	V	
16M w/ RPMC	UC6	WSON8	CS1#	V	
32M w/ RPMC	UC2	WSON8	CS0#		V

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MCP4/13/SPI,SMB,ESPI

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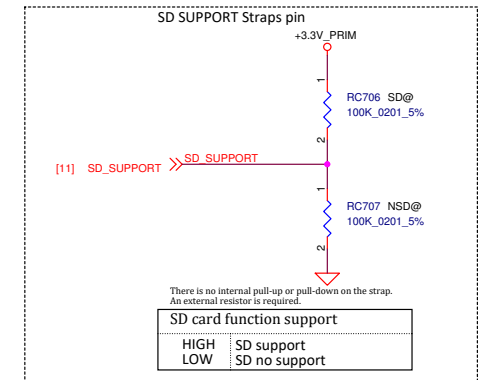
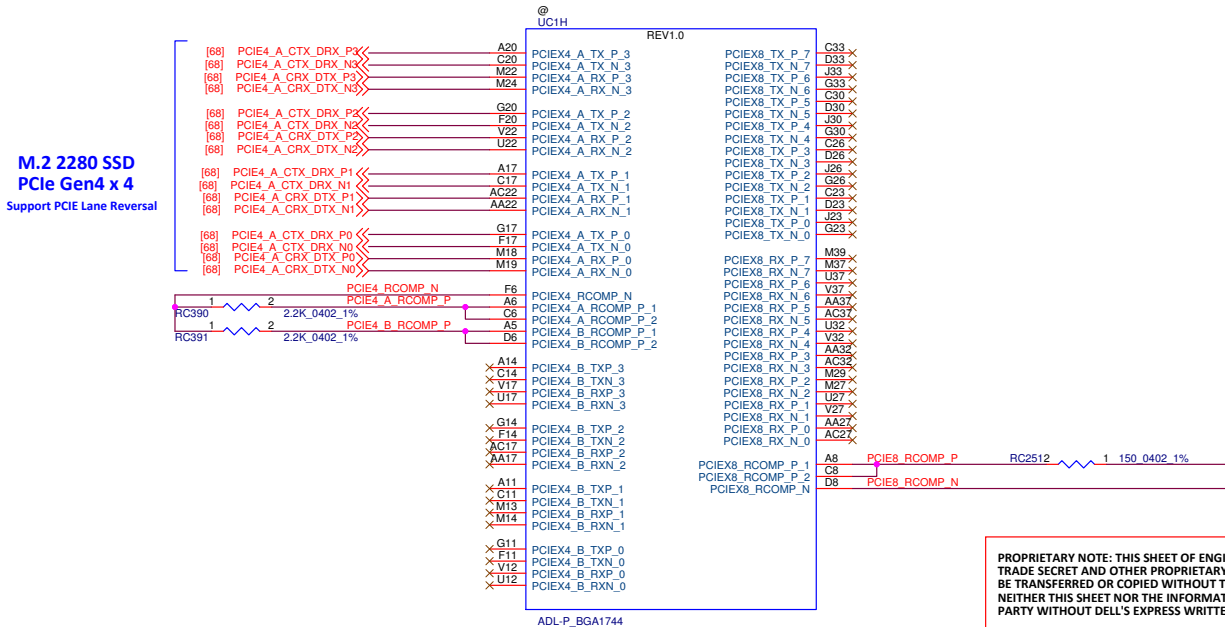
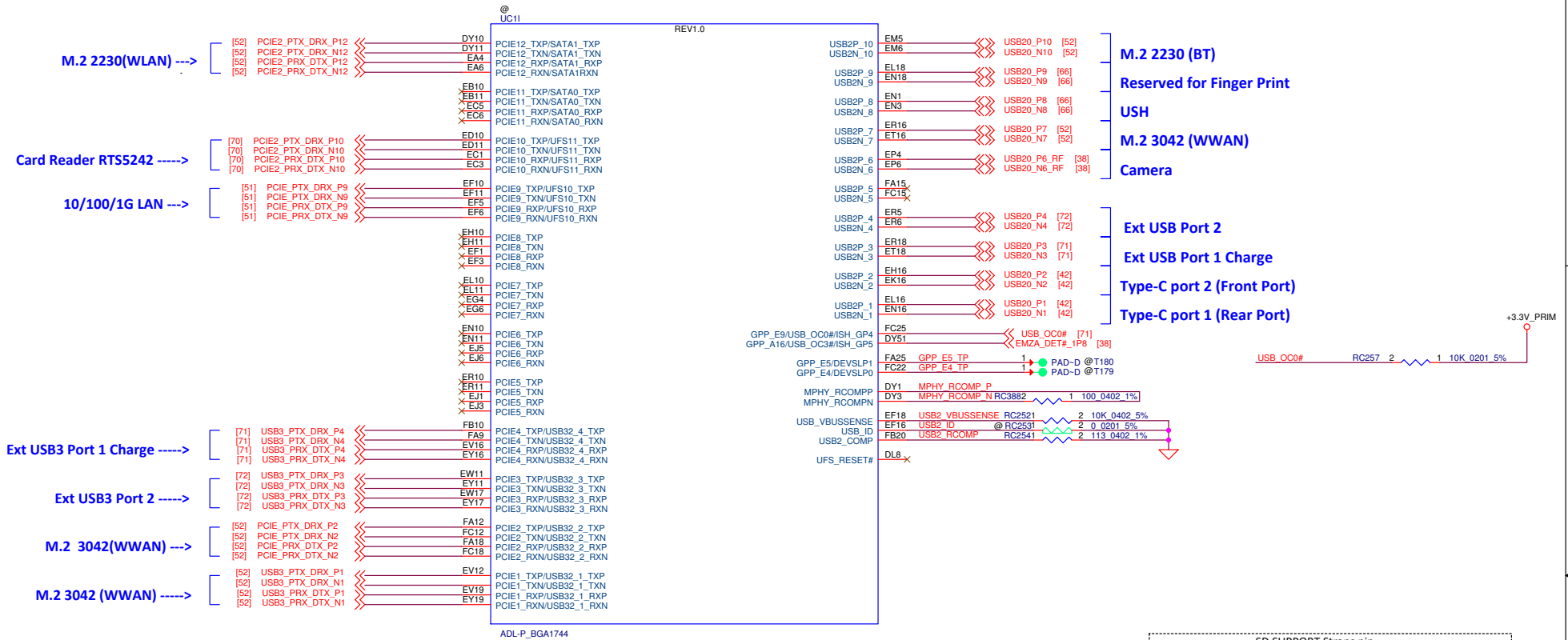
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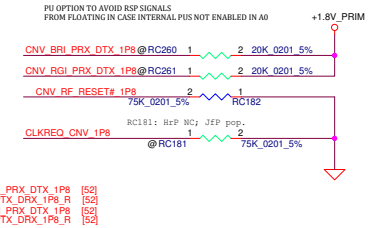
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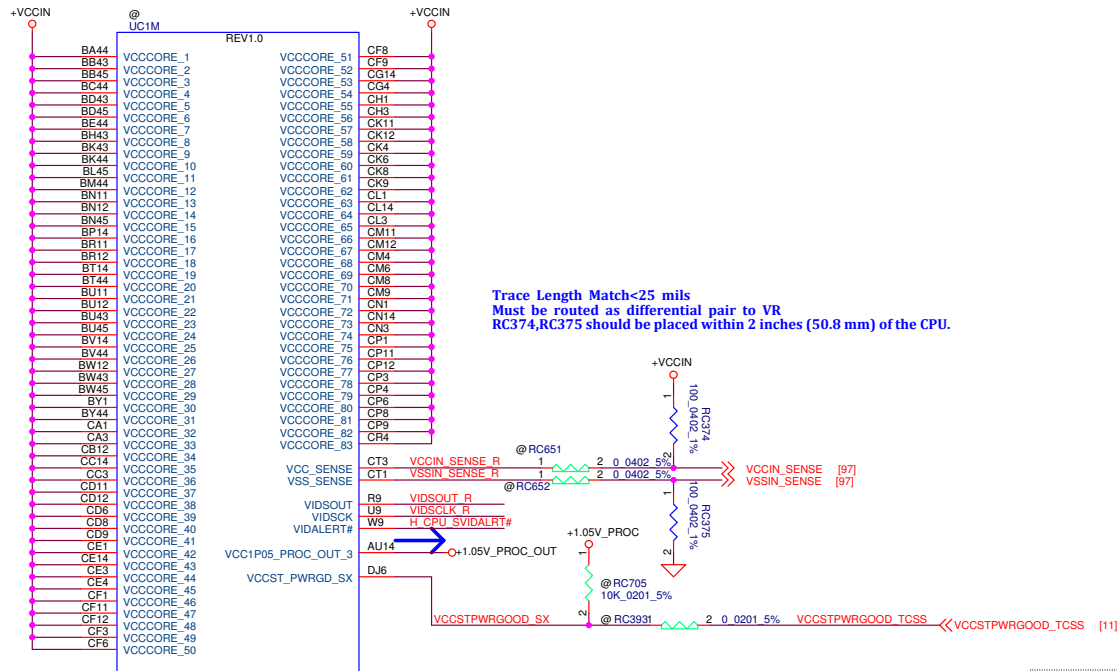
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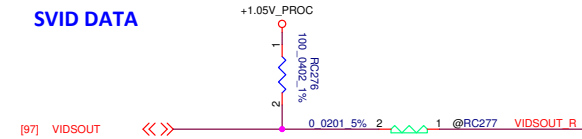


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	Size	Document Number	Rev
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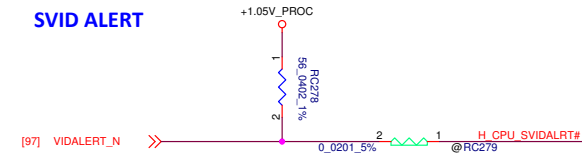


- 1.The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
 - 2.Route the Alert signal between the Clock and the Data signals.
- CAD Note: Place the PU resistors close to CPU

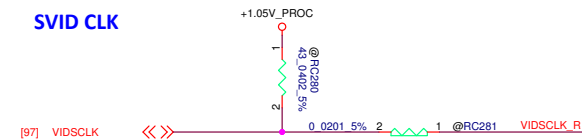
SVID DATA



SVID ALERT



SVID CLK

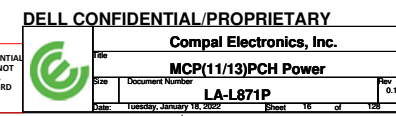


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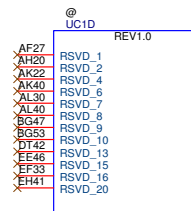
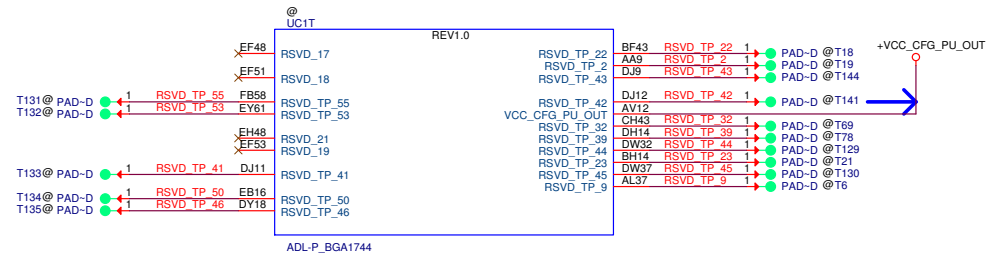
@ UC1P			REV1.0			AL15		
A3	VSS_7	VSS_74	AL17					
A10	VSS_75	AL22						
A21	VSS_2	VSS_76	AL4					
A23	VSS_3	VSS_77	AL41					
A26	VSS_4	VSS_78	AL54					
A28	VSS_5	VSS_79	AM11					
A30	VSS_6	VSS_80	AM1					
A31	VSS_8	VSS_81	AM51					
A33	VSS_9	VSS_82	AM55					
A40	VSS_10	VSS_83	AM9					
A47	VSS_11	VSS_84	AN17					
A48	VSS_12	VSS_85	AN10					
A60	VSS_13	VSS_86	AN46					
AA11	VSS_14	VSS_87	AN48					
AA12	VSS_15	VSS_88	AN58					
AA26	VSS_16	VSS_89	BL4					
AA31	VSS_17	VSS_90	AP15					
AA35	VSS_18	VSS_91	AP20					
AA40	VSS_19	VSS_92	AP22					
AA44	VSS_20	VSS_93	AP25					
AA57	VSS_21	VSS_94	AP35					
AA59	VSS_22	VSS_95	AP51					
AB16	VSS_23	VSS_96	AP55					
AB21	VSS_24	VSS_97	AP9					
AB26	VSS_25	VSS_98	AR4					
AB31	VSS_26	VSS_99	AR54					
AB35	VSS_27	VSS_100	AT47					
AB37	VSS_28	VSS_101	AT57					
AB44	VSS_29	VSS_102	AT59					
AC40	VSS_30	VSS_103	AT6					
AC44	VSS_31	VSS_104	AT8					
AC51	VSS_32	VSS_105	AU54					
AC55	VSS_33	VSS_106	AV11					
AC6	VSS_34	VSS_107	AV4					
AC8	VSS_35	VSS_108	AV9					
AD21	VSS_36	VSS_109	AW1					
AD26	VSS_37	VSS_110	AW14					
AD31	VSS_38	VSS_111	AW51					
AD35	VSS_39	VSS_112	AW55					
AD48	VSS_40	VSS_113	AY1					
AD48	VSS_41	VSS_114	AY43					
AD58	VSS_42	VSS_115	AY46					
AE12	VSS_43	VSS_116	AY48					
AE17	VSS_44	VSS_117	AY51					
AE22	VSS_45	VSS_118	AY55					
AE27	VSS_46	VSS_119	AY58					
AE32	VSS_47	VSS_120	AY9					
AE37	VSS_48	VSS_121	B34					
AE40	VSS_49	VSS_122	B4					
AE44	VSS_50	VSS_123	B43					
AE52	VSS_51	VSS_124	B50					
AE9	VSS_52	VSS_125	B58					
AF4	VSS_53	VSS_126	B61					
	VSS_54	VSS_127						
	VSS_55	VSS_128	BB12					
AG1	VSS_56	VSS_130	BB54					
AG51	VSS_57	VSS_131	BB6					
AG58	VSS_58	VSS_132	BB8					
AH9	VSS_59	VSS_133	BB9					
AJ3	VSS_60	VSS_134	BC14					
AJ41	VSS_61	VSS_135	BC47					
AJ47	VSS_62	VSS_136	BC57					
AJ49	VSS_63	VSS_137	BC59					
AK25	VSS_64	VSS_138	BD4					
AK20	VSS_65	VSS_139	BD54					
AK30	VSS_66	VSS_140						
AK37	VSS_67	VSS_141	BE12					
AK4	VSS_68	VSS_143	BE51					
AK4	VSS_69	VSS_144	BE55					
AK57	VSS_70	VSS_145	BE9					
AK59	VSS_71	VSS_146	BF46					
AK9	VSS_72	VSS_147	BF48					
	VSS_73	VSS_148						

ADL-P_BGA1744

@ UC1Q			REV1.0			CD58		
BF58	VSS_149	VSS_222	CE51					
BG1	VSS_150	VSS_223	CE55					
BG12	VSS_151	VSS_224	CF47					
BG44	VSS_152	VSS_225	CF49					
BG52	VSS_153	VSS_226	CF54					
BG9	VSS_154	VSS_227	CG57					
BH4	VSS_155	VSS_228	CG59					
BH46	VSS_156	VSS_229	CH11					
BH48	VSS_157	VSS_230	CH12					
BH58	VSS_158	VSS_231	CH54					
BL51	VSS_159	VSS_232	CH8					
BL55	VSS_160	VSS_233	CH9					
BL5	VSS_161	VSS_234	CH19					
BL9	VSS_162	VSS_235	CJ14					
BL11	VSS_163	VSS_236	CJ4					
BL4	VSS_164	VSS_237	CJ44					
BL54	VSS_165	VSS_238	CK1					
BL9	VSS_166	VSS_239	CK3					
BL14	VSS_167	VSS_240	CK46					
BM1	VSS_168	VSS_241	CK43					
BM14	VSS_169	VSS_242	CK48					
BM47	VSS_170	VSS_243	CK51					
BM57	VSS_171	VSS_244	CK55					
BM59	VSS_172	VSS_245	CK58					
BN1	VSS_173	VSS_246	CM52					
BN54	VSS_174	VSS_247	CM59					
BN9	VSS_175	VSS_248	CM58					
BP4	VSS_176	VSS_249	CM51					
BP51	VSS_177	VSS_250	CP55					
BP55	VSS_178	VSS_251	CR43					
BR43	VSS_179	VSS_252	CR47					
BR48	VSS_180	VSS_253	CR49					
BR58	VSS_181	VSS_254	CR54					
BR6	VSS_182	VSS_255	CT11					
BR8	VSS_183	VSS_256	CT57					
BR9	VSS_184	VSS_257	CT59					
BT4	VSS_185	VSS_258	CT6					
BT51	VSS_186	VSS_259	CT8					
BT55	VSS_187	VSS_260	CT9					
BU54	VSS_188	VSS_261	CU4					
BU9	VSS_189	VSS_262	CU54					
BV1	VSS_190	VSS_263	CV14					
BV47	VSS_191	VSS_264	CW43					
BV57	VSS_192	VSS_265	CW46					
BV59	VSS_193	VSS_266	CW48					
BW4	VSS_194	VSS_267	CW51					
BW54	VSS_195	VSS_268	CW55					
BW9	VSS_196	VSS_269	CW58					
BY3	VSS_197	VSS_270	CY51					
C1	VSS_198	VSS_271	CY55					
C21	VSS_199	VSS_272	D11					
C25	VSS_200	VSS_273	D14					
C28	VSS_201	VSS_274	D17					
	VSS_202	VSS_275	D20					
	VSS_203	VSS_276	D21					
C34	VSS_204	VSS_277	D25					
C40	VSS_205	VSS_278	D28					
C47	VSS_206	VSS_279	D31					
C9	VSS_207	VSS_280	D4					
CA14	VSS_208	VSS_281	D53					
CA43	VSS_209	VSS_282	D56					
CA46	VSS_210	VSS_283	D58					
CA48	VSS_211	VSS_284	D59					
CA51	VSS_212	VSS_285	D9					
CA55	VSS_213	VSS_286	DA11					
CA58	VSS_214	VSS_287	DA12					
CB4	VSS_215	VSS_288	DA6					
CB6	VSS_216	VSS_289	DA8					
CB8	VSS_217	VSS_290	DB14					
CB9	VSS_218	VSS_291	DB4					
CC1	VSS_219	VSS_292	DB54					
CC52	VSS_220	VSS_293						
CD46	VSS_221	VSS_294						

ADL-P_BGA1744

@ UC1R			REV1.0					
DC47	VSS_295	VSS_369	EE58					
DC54	VSS_296	VSS_370	ED6					
DC57	VSS_297	VSS_371	ED60					
DC59	VSS_298	VSS_372	EE16					
DE44	VSS_299	VSS_373	EE43					
DE51	VSS_300	VSS_374	EE51					
DE55	VSS_301	VSS_375	EE13					
DF43	VSS_302	VSS_376	EE8					
DF46	VSS_303	VSS_377	EH13					
DF48	VSS_304	VSS_378	EH8					
DF58	VSS_305	VSS_379	EH2					
DG11	VSS_306	VSS_380	FK28					
DG12	VSS_307	VSS_381	FK36					
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DG6	VSS_310	VSS_384	FK58					
DG8	VSS_311	VSS_385	EL3					
DG9	VSS_312	VSS_386	EL4					
DH4	VSS_313	VSS_387	EL6					
DH54	VSS_314	VSS_388	EL8					
DJ47	VSS_315	VSS_389	EN13					
DJ57	VSS_316	VSS_390	EN8					
DJ59	VSS_317	VSS_391	EN14					
DK14	VSS_318	VSS_392	ER1					
DK54	VSS_319	VSS_393	ER13					
DL10	VSS_320	VSS_394	ER21					
DL11	VSS_321	VSS_395	ER28					
DL13	VSS_322	VSS_396	ER3					
DM4	VSS_323	VSS_397	ER36					
DM41	VSS_324	VSS_398	ER43					
DM46	VSS_325	VSS_399	ER51					
DM48	VSS_326	VSS_400	ER6					
DM51	VSS_327	VSS_401	ER8					
DM55	VSS_328	VSS_402	EU11					
DM58	VSS_329	VSS_403	EU36					
DM6	VSS_330	VSS_404	EU58					
DM61	VSS_331	VSS_405	EU8					
DN13	VSS_332	VSS_406	EV14					
DN8	VSS_333	VSS_407	EV20					
DP46	VSS_334	VSS_408	EV26					
DP49	VSS_335	VSS_409	EV33					
DT13	VSS_336	VSS_410	EV39					
DT52	VSS_337	VSS_411	EV4					
DT8	VSS_338	VSS_412	EV45					
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DV49	VSS_343	VSS_417	EV14					
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DV58	VSS_345	VSS_419	EV26					
DV6	VSS_346	VSS_420	EV3					
DV8	VSS_347	VSS_421	EV33					
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EB31	VSS_361	VSS_434	F38					
EB8	VSS_362	VSS_435	F40					
EC11	VSS_363	VSS_436	F43					
EC21	VSS_364	VSS_437	F44					
EC28	VSS_365	VSS_438	F30					
ED1	VSS_366	VSS_439	F47					
ED4	VSS_367	VSS_440	F46					
ED56	VSS_368	VSS_441	F47					



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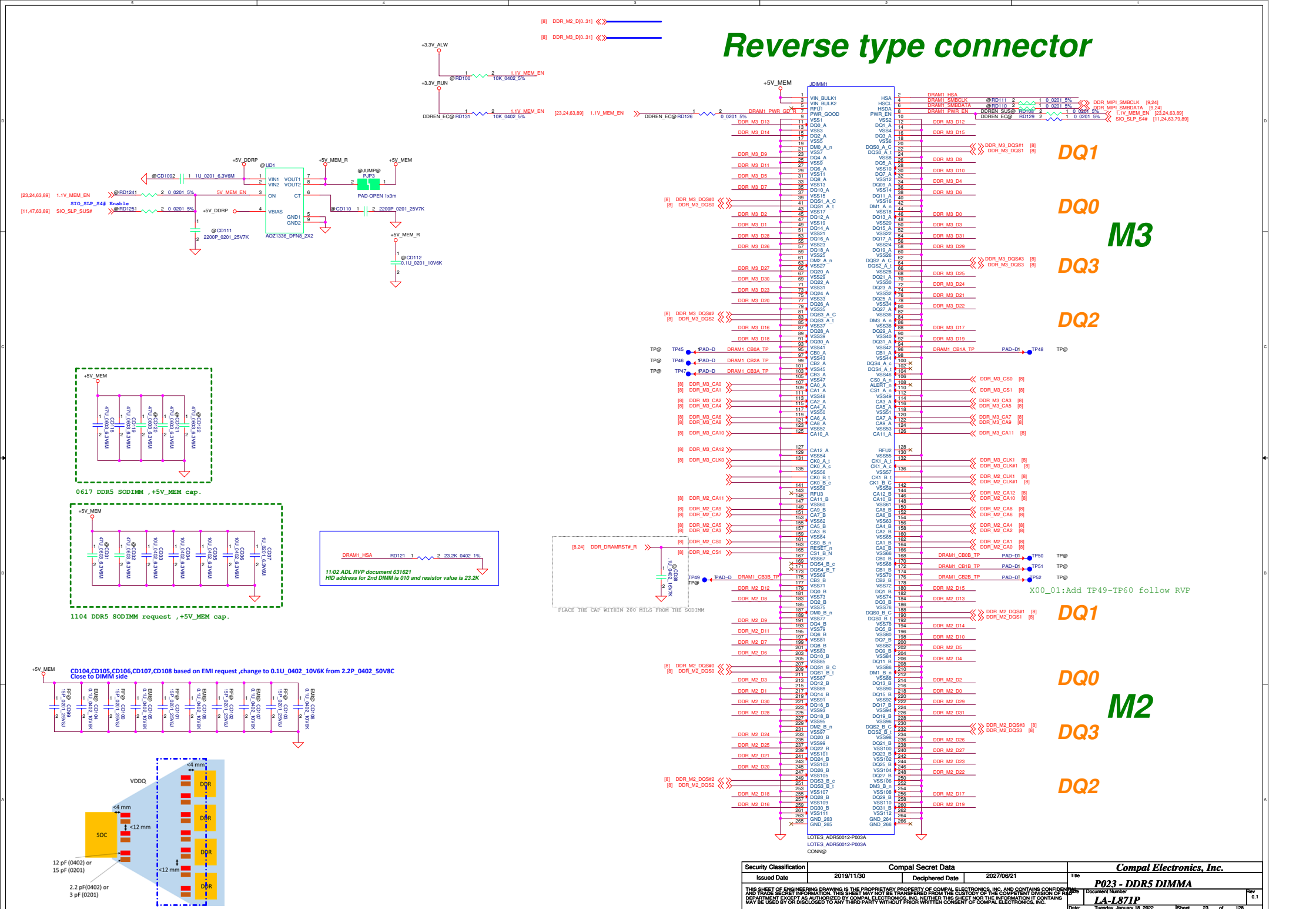
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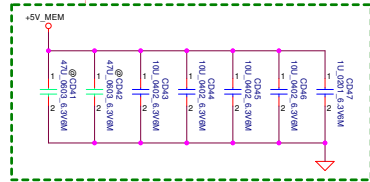
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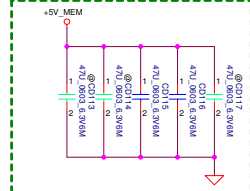
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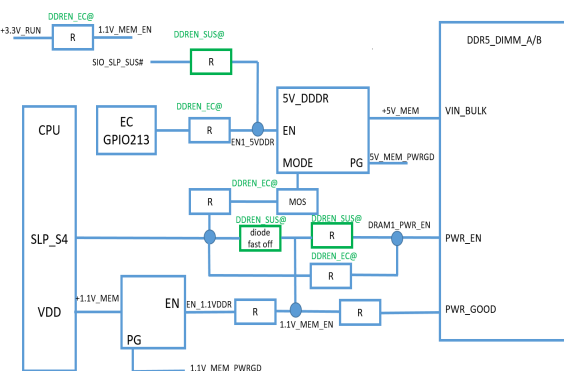
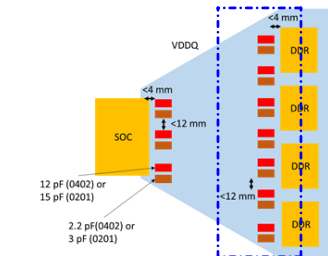
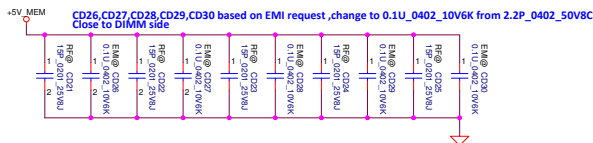
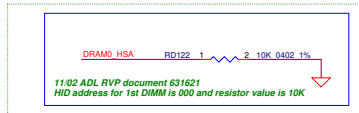
Layout Note:
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1104 DDR5 SODIMM request ,+5V_MEM cap.
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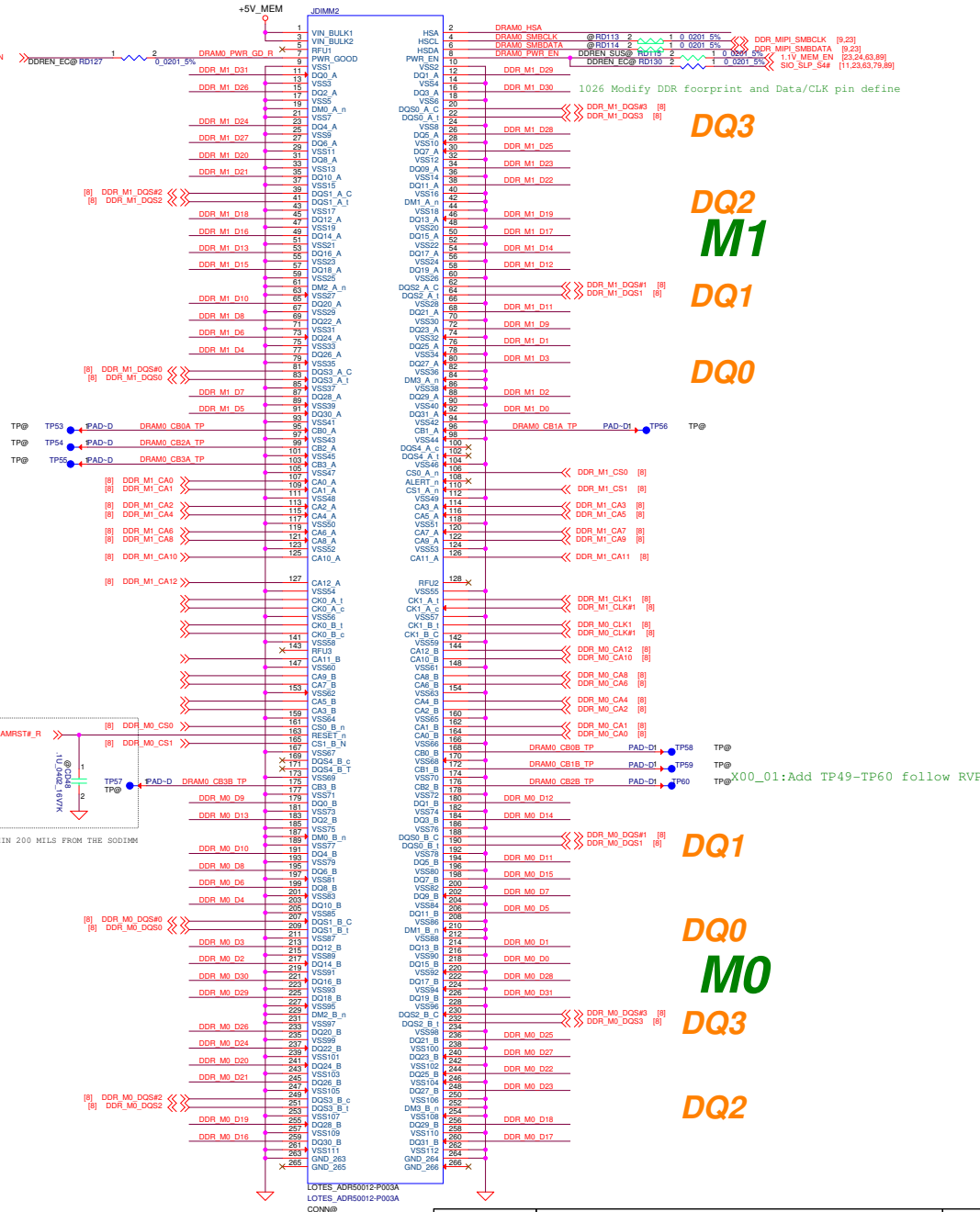


0617 DDR5 SODIMM ,+5V_MEM cap.



```
1103 Del SODIMM DDR4 Vref pin
DDR5 VREF doesn't to connect to CPU
```

Reverse type connector



Security Classification	Compal Secret Data			Title	
Issued Date	2019/11/30	Deciphered Date	2027/06/21	P024 - DDR5 DIMMB Document Number LA-1871P	
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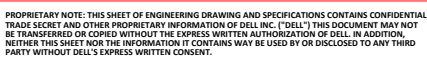
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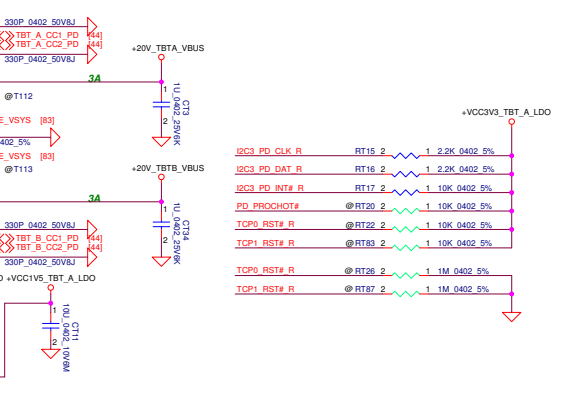
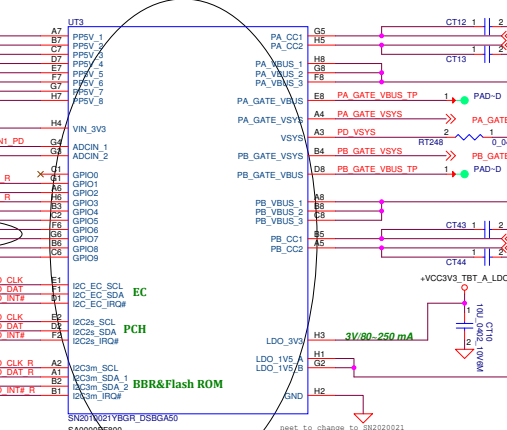
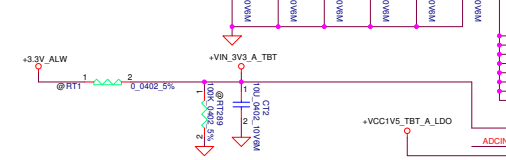
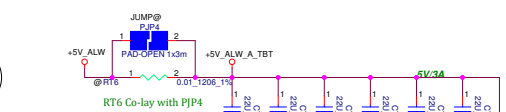
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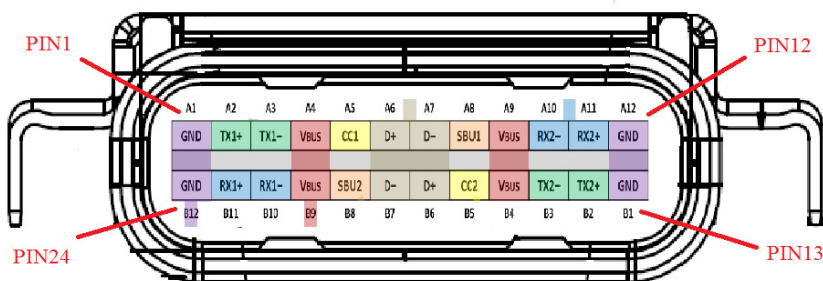
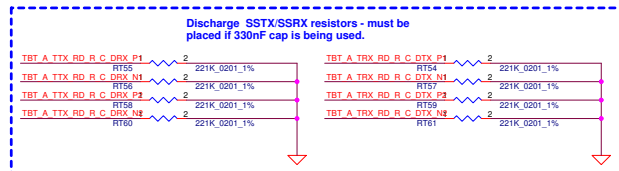
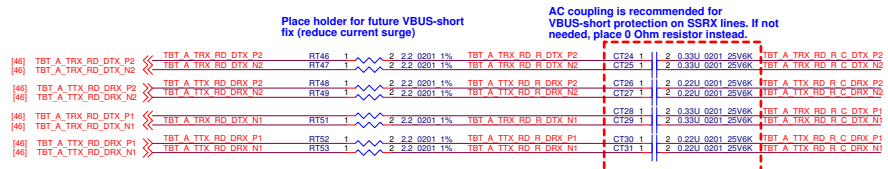
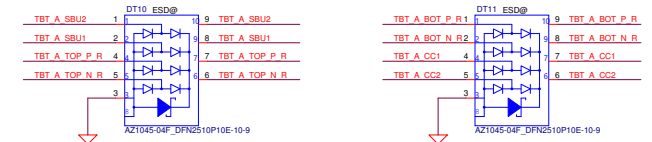
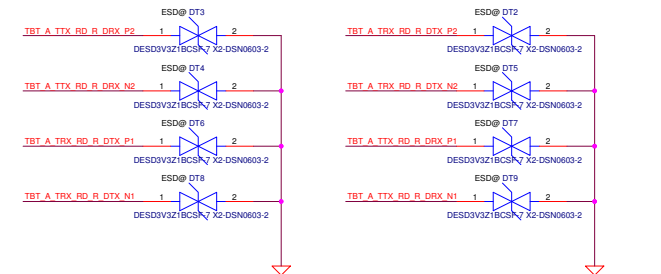
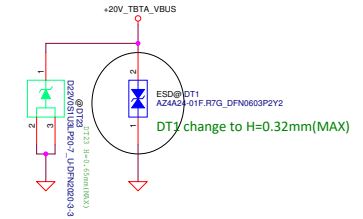
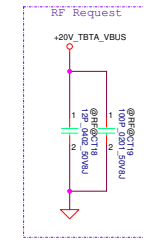
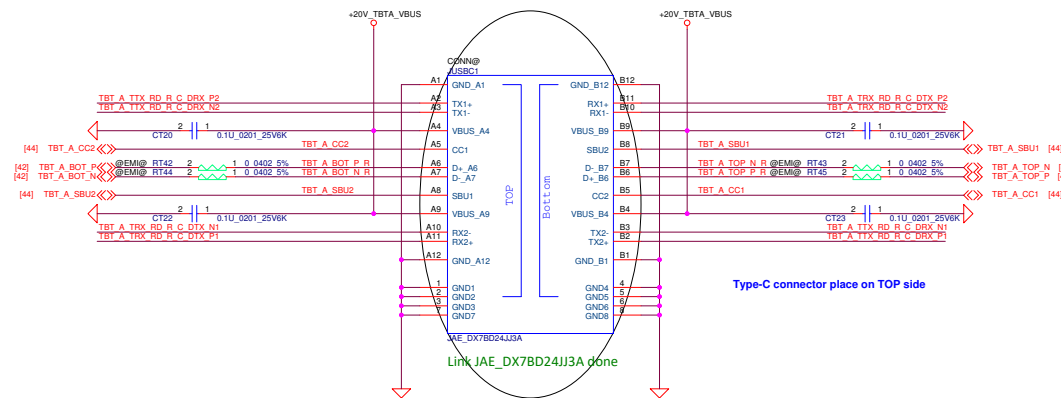
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need to change to SN2020021



For Type-C port 1(No support DDM)



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[TypeC]Connector Port1

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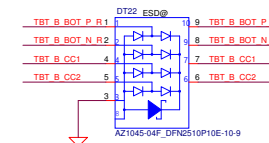
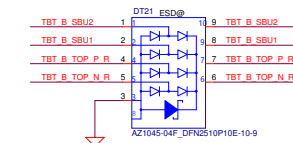
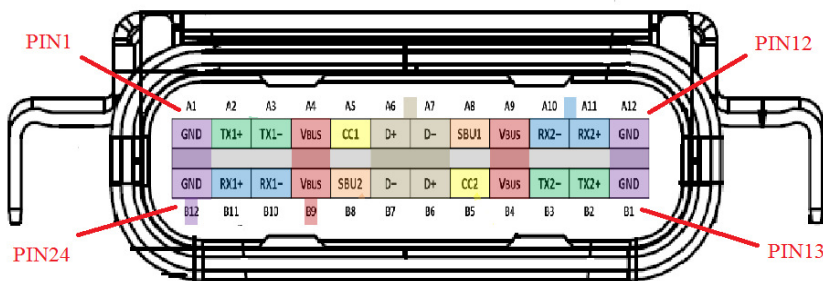
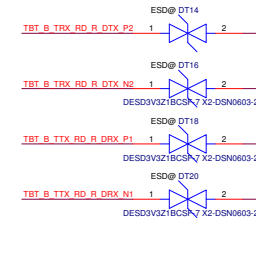
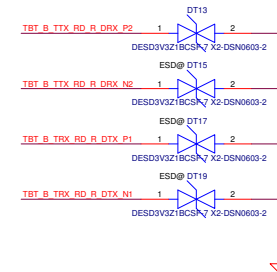
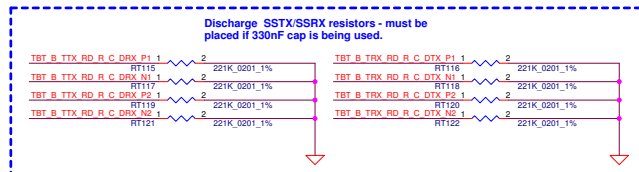
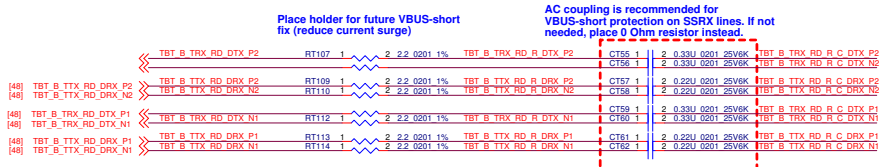
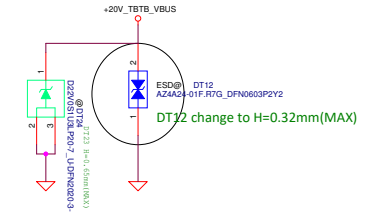
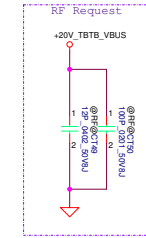
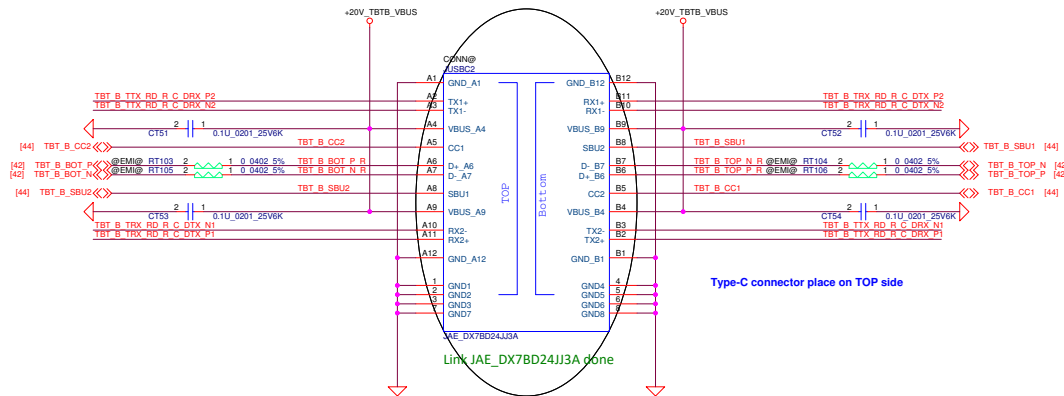
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Title			
TypeC Connector Port1			
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For Type-C port 2(No support DDM)

JAE X12 DX07BD24JJ3 with X10 DX07BD24JJ2 same layout



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[TypeC]Connector Port2				Rev
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From CPU

TBT PORTS

BB@UT10

Port A - Host Side
Port B - Type-C Side

JHL8040R-SLMN7-A1_BGA105-D

To Type-C Port1 connector

MISC & DEBUG

BB@UT1A

JHL8040R-SLMN7-A1_BGA105-D

RT ref p.5 XTAL Recommended
FW2500025Z by Pericom
XRCGB25M000F3L12R0 by Murata
Suggest adding GND shield across
Crystal and 18pF caps for better
RFI.

PD

SMBUS to PCH SML0 for vPRO Support

PCH

(L11) DG_P1_RST#:
For PD based systems, DG_P1_RST# should be output from PD.
For TCPC based systems, DG_P1_RST# should be output from SOC/EC.

(B10) FORCE_PWR: Connect to PCH for FW update
'0' - by default
'1' - for debug only

(A8) DG_FLASH_BUSY#: connection to PU

(A4) DG_FLASH_SHARE_EN (iPU):
'0' - Flash isn't shared. 1 Flash per Re-timer. Can be left NC.
'1' - Flash is shared between 2 Re-timers.

(A5) DG_FLASH_MSTR_SLV (iPU):
'0' - Set Re-timer to be Slave on shared flash SPI I/F.
'1' - Set Re-timer to be Master on shared flash SPI I/F.

(A8) DG_POC_GPIO6:
'0' - Reserved for debug
'1' - Indication to S0 state for Re-timer

BBR ROM choice need follow Intel approved list

3.1 Flash Types Supported

Table 12. Supported Types of Flash Memory

Manufacturer	Type	Volume, Mbit	Supply, V
AMIC	A25L080	8.0	3.0-3.6
Spansion	S25FL208K	8.0	2.7-3.6
Winbond	W25Q80GVNSIG	8.0 (8pin SOIC150 mil)	2.7-3.6
Macronix	MX25L8006EM11	8.0 (150mil, 8-SOP)	2.7-3.6
Micron	M25PE80-VMM6TP	8.0 (150mil, SO8N)	2.7-3.6
Micron	M25PX80-VMM6TP	8.0 (150mil, SO8N)	2.7-3.6

JTAG Debug

For BBR-0 ALL Issue Workaround reserved

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[TypeC]TBT BB TCSS Port1

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From CPU

TBT PORTS

To Type-C Port2 connector

MISC & DEBUG

POC_GPIO_12 have iPU

SMBUS to PCH SML0 for vPRO Support

PCH

- Flash Sharing between 2 Re-timers:
- * SPI signals should be shared (DG_EE_DI, DG_EE_DO, DG_EE_CS#, DG_EE_CLK)
 - * DG_FLASH_BUSY# should be shared between BBR#1 and BBR#2 with PU to PW_VCC3v3, SX_SYS
 - * DG_FLASH_MSTR_SLV of BBR#1 (set as Master) should be PU and PD for BBR#2 (set as Slave)
 - * DG_FLASH_SHARE_EN should be PU.

TBT BB Flash ROM sharing

- [46] TBT_SHR_ROM_DI << @RT2492 1 0 0402 5% TBT_B_ROM_DI
- [46] TBT_SHR_ROM_DO << @RT2502 1 0 0402 5% TBT_B_ROM_DO
- [49] TBT_SHR_ROM_CLK << @RT2522 1 0 0402 5% TBT_B_ROM_CLK

JTAG Debug

For BBR-A0 PLL Issue Workaround reserved

- TBT_B_JTAG_TDI RT227 1 2 10K 0201 5%
- TBT_B_JTAG_TCK RT228 1 2 10K 0201 5%
- TBT_B_JTAG_TMS RT230 1 2 10K 0201 5%
- TBT_B_JTAG_TDO RT231 1 2 10K 0201 5%

(L11) DG_P1_RST#:

For PD based systems, DG_P1_RST# should be output from PD.

For TCPC based systems, DG_P1_RST# should be output from SOC/EC.

(B10) FORCE_PWR: Connect to PCH for FW update

'0' - by default

'1' - for debug only

(A9) DG_FLASH_BUSY#: connection to PU

(A4) DG_FLASH_SHARE_EN (iPU):

'0' - Flash isn't shared. 1 Flash per Re-timer. Can be left NC.

'1' - Flash is shared between 2 Re-timers.

(A5) DG_FLASH_MSTR_SLV (iPU):

'0' - Set Re-timer to be Slave on shared flash SPI I/F.

'1' - Set Re-timer to be Master on shared flash SPI I/F.

(A8) DG_POC_GPIO6:

'0' - Reserved for debug

'1' - Indication to S0 state for Re-timer

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TypeC/TBT BB TCSS Port2

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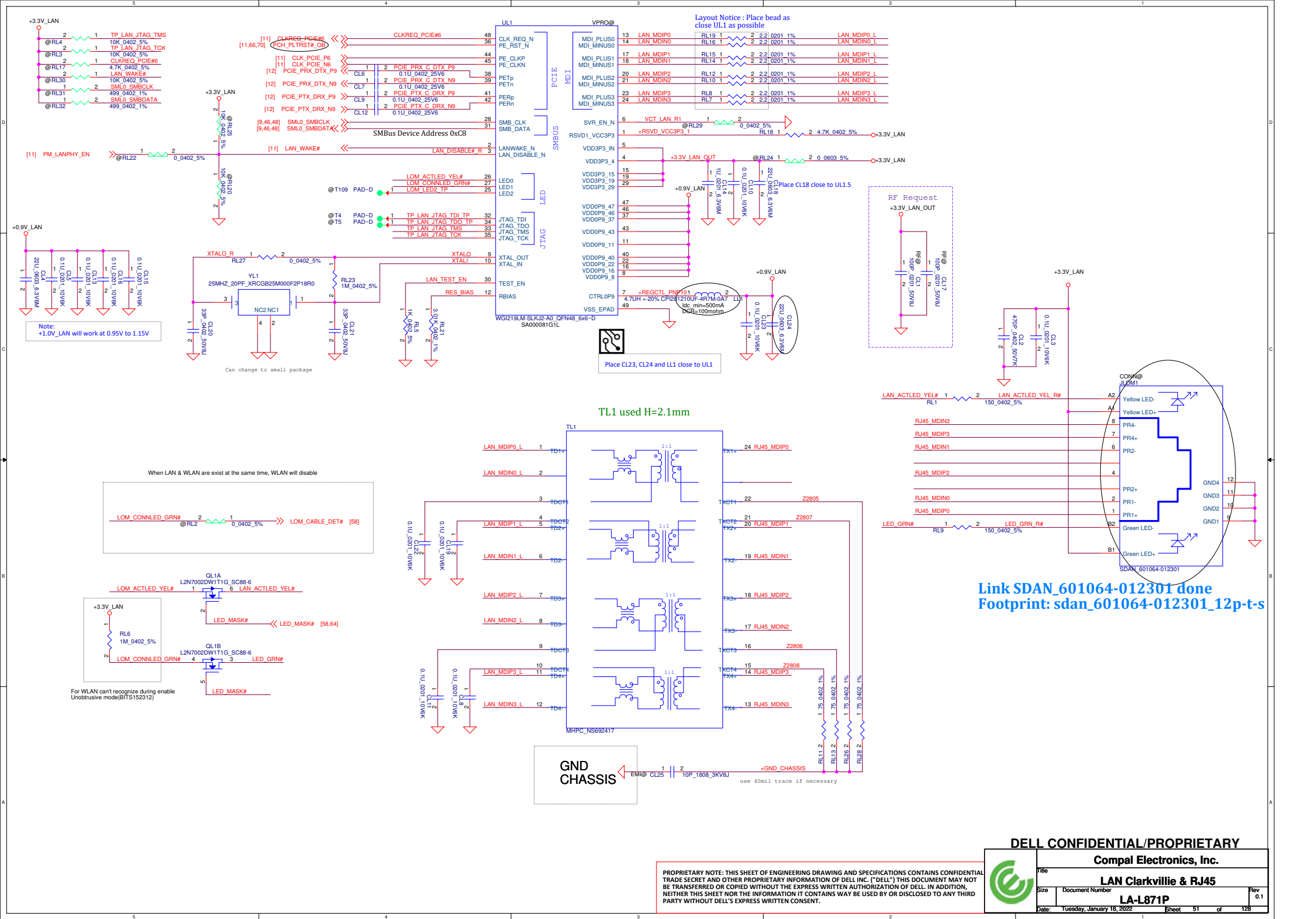
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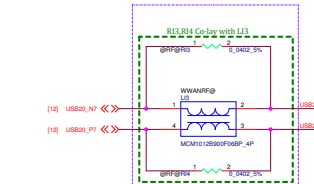
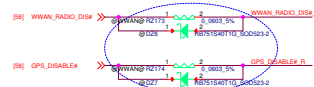
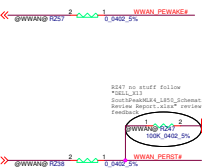
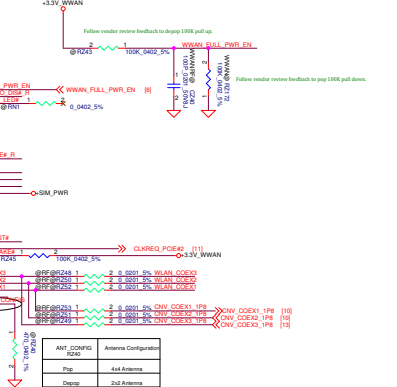
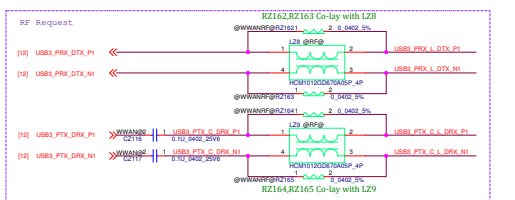
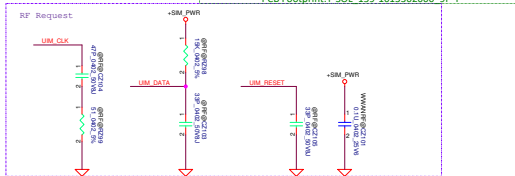
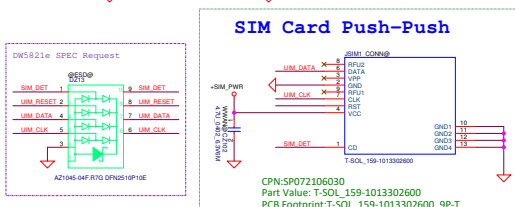
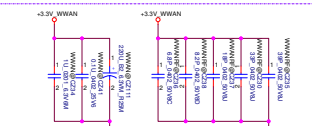
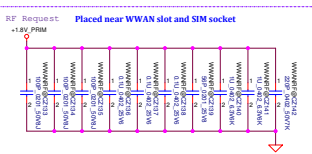
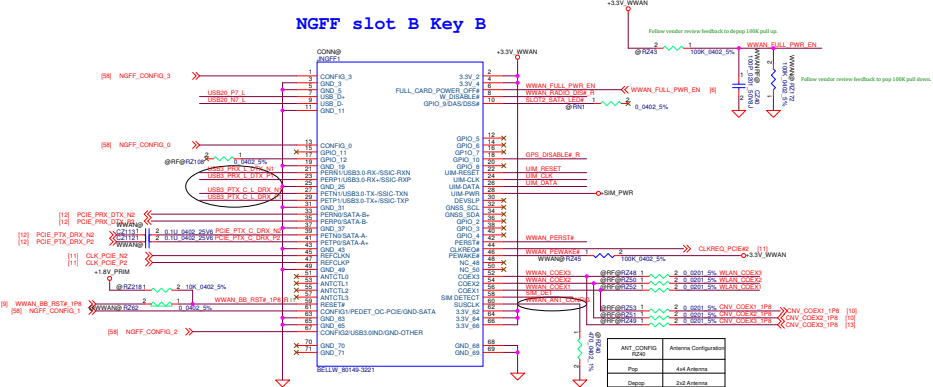
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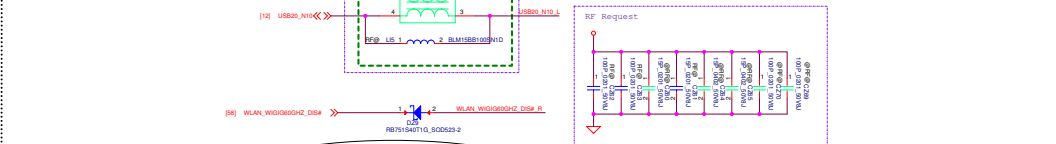
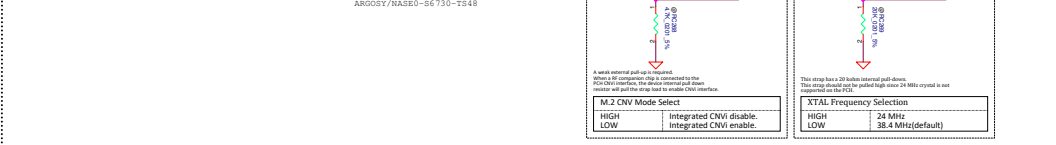
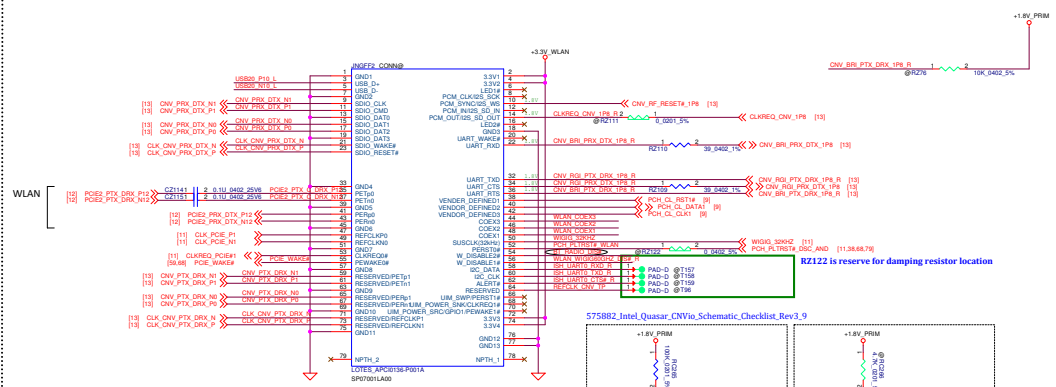
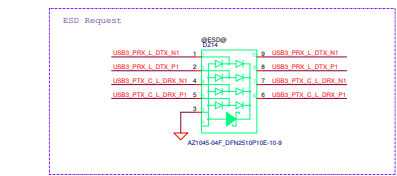
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Reserve [Type C]PD Power		
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NGFF slot B Key B



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
	GND	GND	GND	GND	SSD_SATA
	GND	HIGH	GND	GND	SSD_PCIE(2 lane)
	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA_PCIE(1 lane)
15	HIGH	HIGH	HIGH	HIGH	NA



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PCIE/SATA DEMUX			
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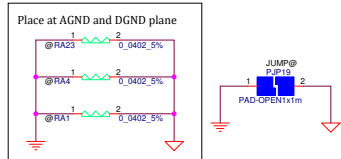
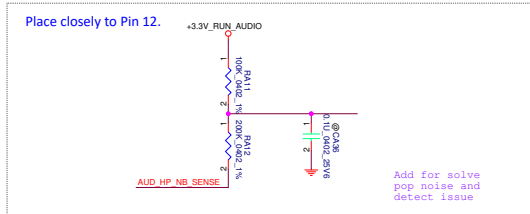
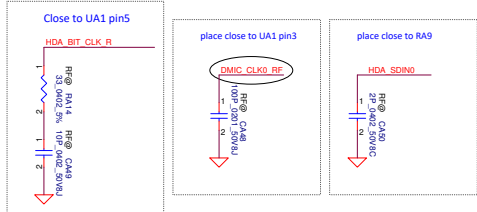
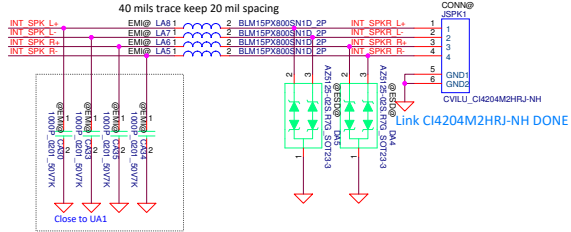


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PCIE device		
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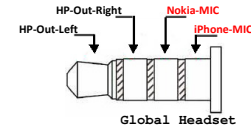
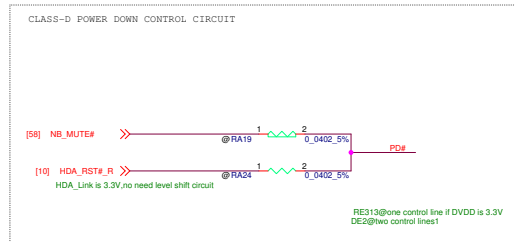
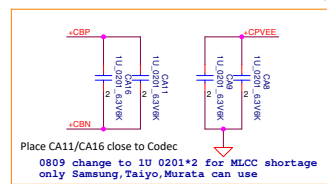
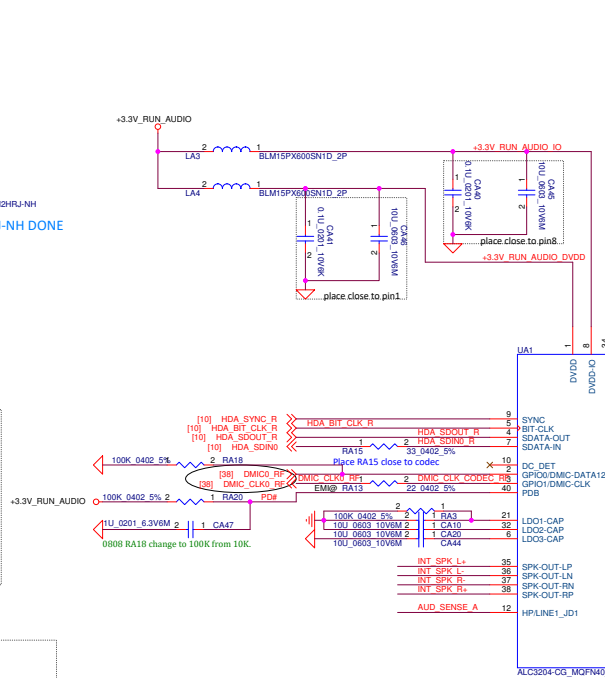
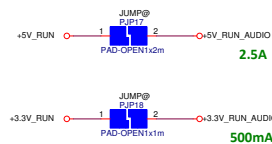
1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box)

Internal Speakers Header

40 mils trace keep 20 mil spacing

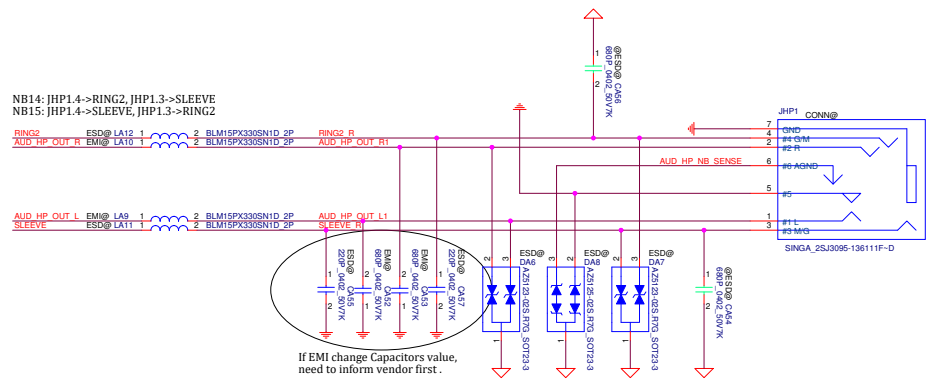


Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN



Universal Jack

Add this Filter to avoid other components/chips too influenced



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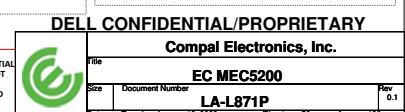
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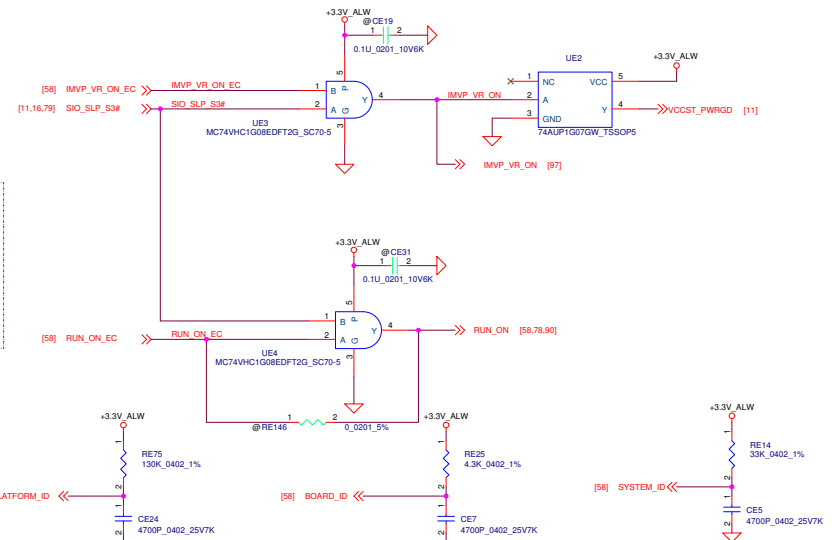
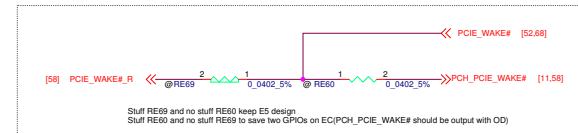
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Audio Amplifier		
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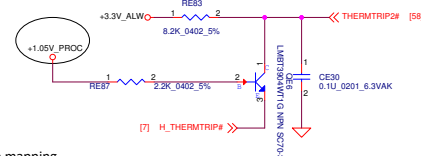


	RE75	CE24	REV
	240K	4700p	
*	130K	4700p	
	62K	4700p	
	33K	4700p	
	8.2K	4700p	AWD-MLK
	4.3K	4700p	
	2K	4700p	
	1K	4700p	

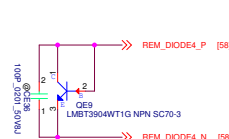
	RE25	CE7	REV
	240K	4700p	X00
	130K	4700p	X01
	62K	4700p	X02
	33K	4700p	X03
	8.2K	4700p	reserve
*	4.3K	4700p	A00
	2K	4700p	
	1K	4700p	

	RE14	CE5	PANEL SIZE
	240K	4700p	11"
	130K	4700p	12"
	62K	4700p	13"
*	33K	4700p	14"
	8.2K	4700p	15"
	4.3K	4700p	17"
	2K	4700p	15P
	1K	4700p	14P

4. SYSTEM_ID rise time is measured from 0%~63.2%.

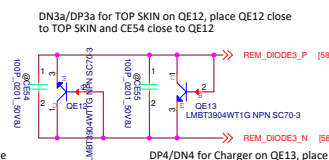


5200 Channel	Location
DP1/DN1	OTP(QE5)
DP2/DN2	Bot Skin(QE11)
DN2a/DP2a	Ambient(QE10)
DP3/DN3	CPU VR(QE9)
DN3a/DP3a	Top Skin(QE12)
DP4/DN4	Charge Choke(OF13)

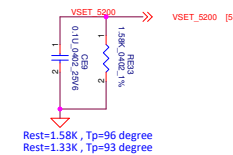


DP2a/DP2a for Ambient on QE10, place QE10 close to Ambient and CE48 close to QE10

DP2/DN2 for Bot skin on QE11, place QE11 close to Bot skin and CE49 close to QE11



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Rest=1.58K , Tp=96 degree
Rest=1.33K , Tp=93 degree

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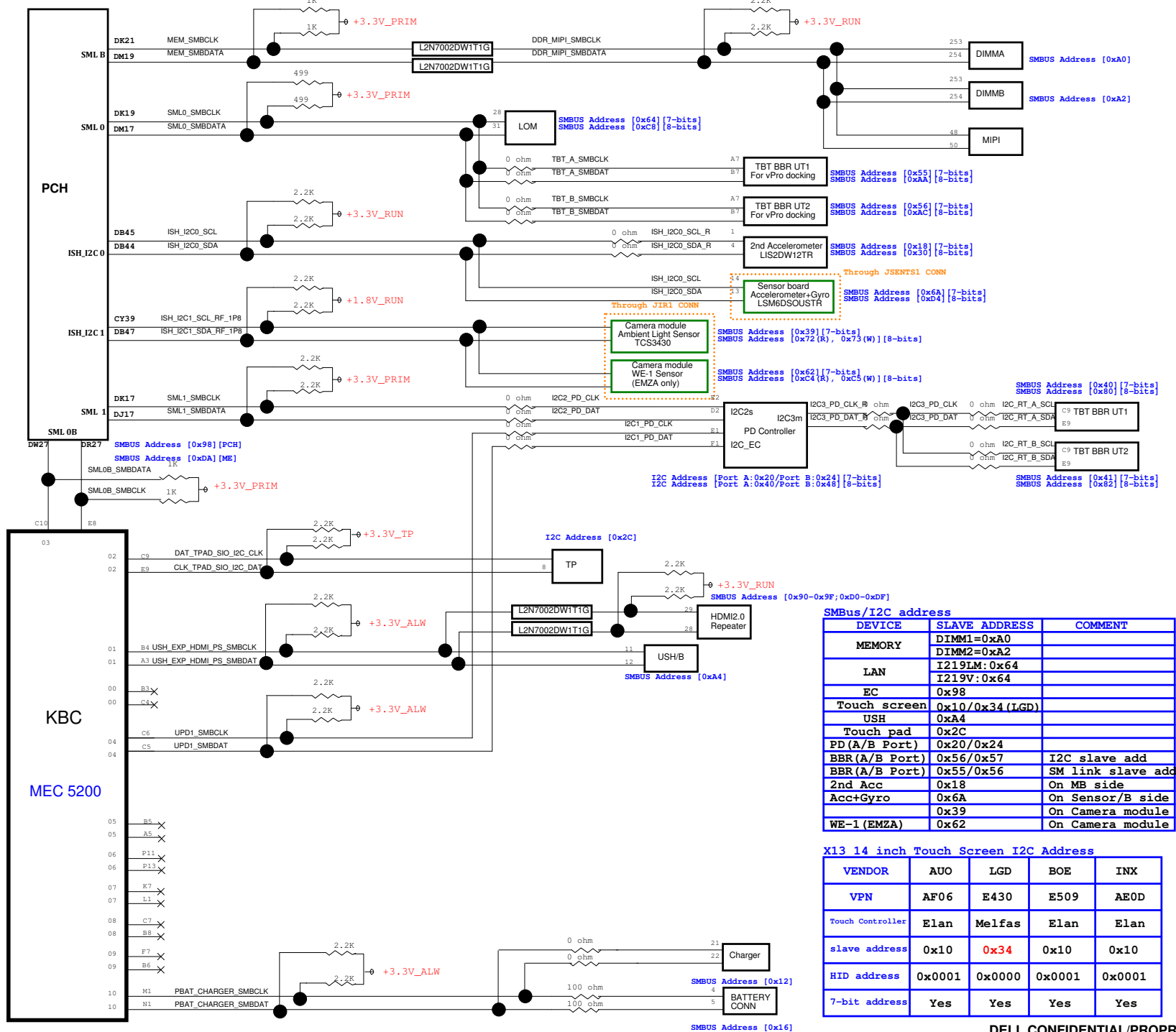
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Secure & Reset IC		
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SMBus/I2C address

DEVICE	SLAVE ADDRESS	COMMENT
MEMORY	DIMM1=0xA0	
	DIMM2=0xA2	
	I219LM:0x64	
LAN	I219V:0x64	
EC	0x98	
Touch screen	0x10/0x34 (LGD)	
USH	0xA4	
Touch pad	0x2C	
PD(A/B Port)	0x20/0x24	
BBR(A/B Port)	0x56/0x57	I2C slave add
BBR(A/B Port)	0x55/0x56	SM link slave add
2nd Acc	0x18	On MB side
Acc+Gyro	0x6A	On Sensor/B side
	0x39	On Camera module
WE-1 (EMZA)	0x62	On Camera module

X13 14 inch Touch Screen I2C Address

VENDOR	AUO	LGD	BOE	INX
VPN	AF06	E430	E509	AE0D
Touch Controller	Elan	Melfas	Elan	Elan
slave address	0x10	0x34	0x10	0x10
HID address	0x0001	0x0000	0x0001	0x0001
7-bit address	Yes	Yes	Yes	Yes

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SMBus Block Diagram

LA-L871P

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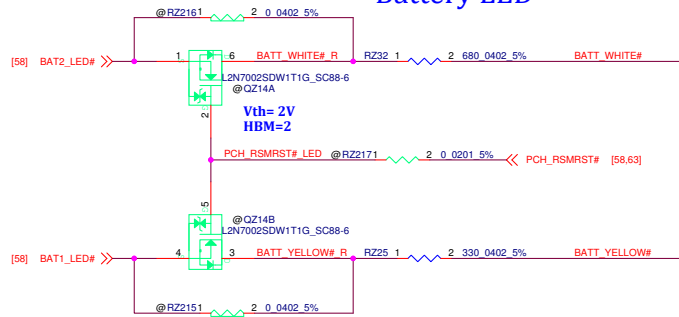
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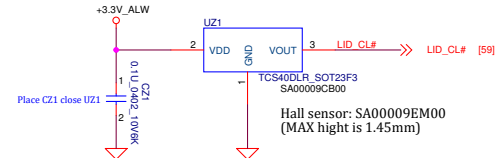


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Compal Electronics, Inc.			
Title			
LED (Controller)			
Size	Document Number		Rev
	LA-L871P		0.1
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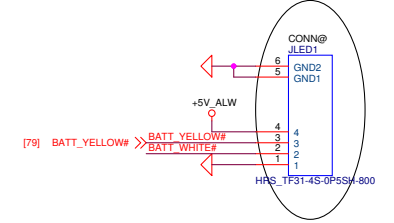
Battery LED



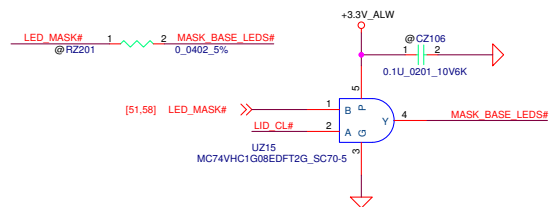
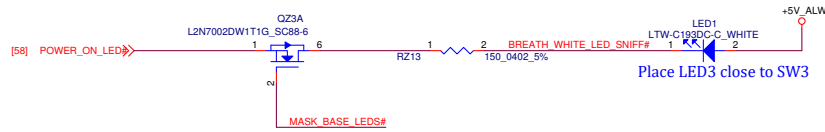
LID SWITCH



LED Board CONN



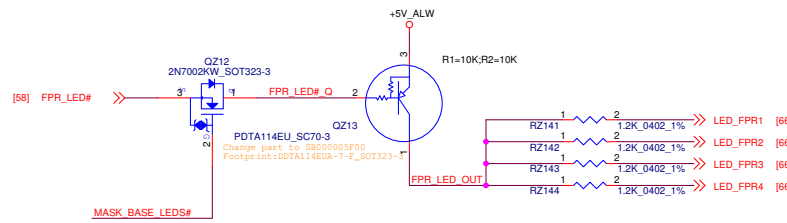
Breath LED



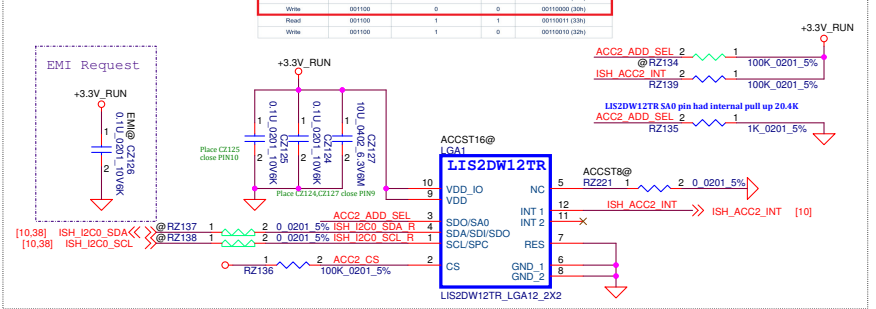
LED Circuit Control Table

	LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

FPR LED



Accelerometer-16bit



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File	LED/Hall Sensor/ACC sensor
Size	Document Number
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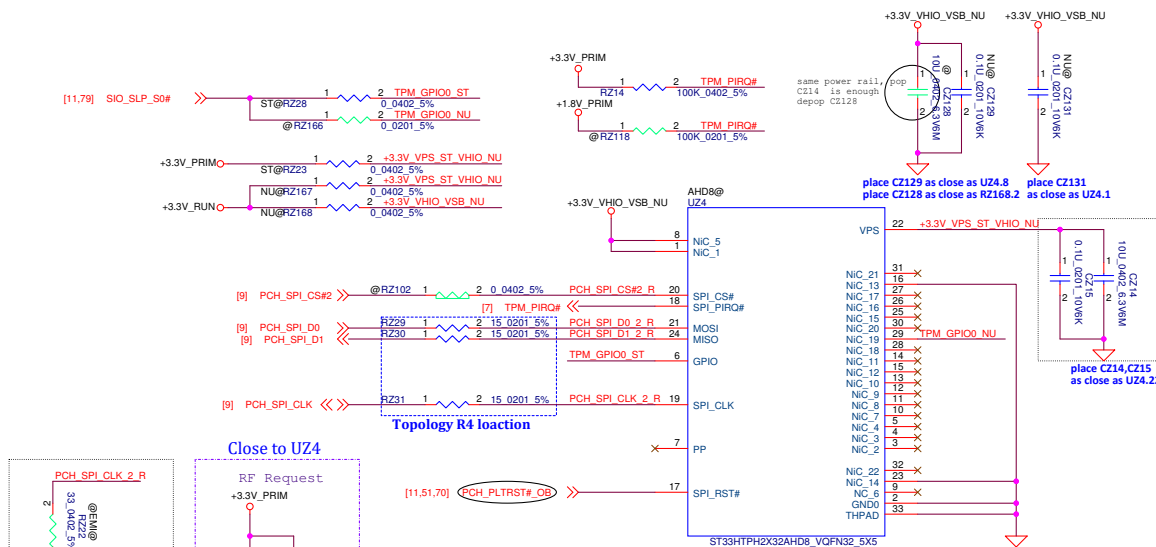


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Title		Reserve for KB/TP/LED/LID	
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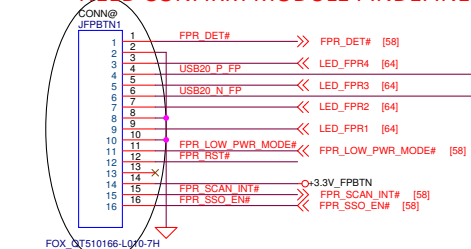
For ST/ Nuvoton TPM



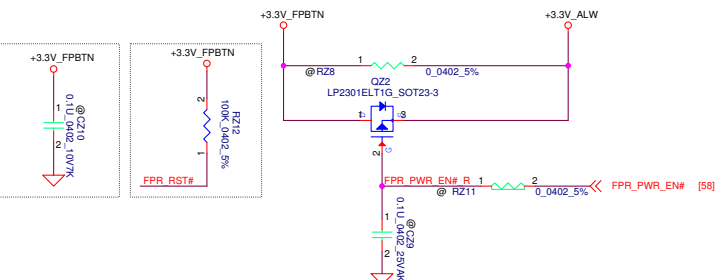
Use ST33HTPH2032AHC1 footprint

FP in PWR BUTTON connector

NEED CONFIRM MODULE PINDEFINE

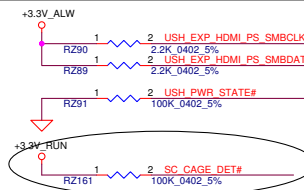
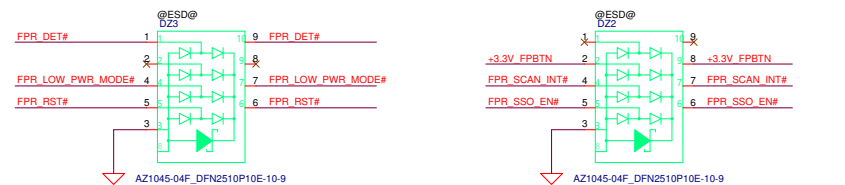


Link FOX_QT510166-L010-7H

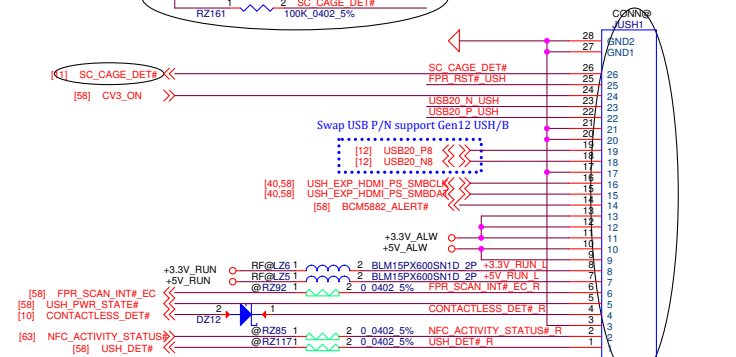


Compal MB CONN Symbol	Signal	FPR Symbol
2	GND	1
4	USB DP(D+)	2
6	USB DM(D-)	3
8	GND	4
10	GND	5
12	FP RESET#	6
14	+3.3V_FPBTN	7
16	FPR_SSO_EN#	8
15	FPR_SCAN_INT#	9
13	N.C	10
11	FPR_LOW_PWR_MODE#	11
9	FPR_LED_1	12
7	FPR_LED_2	13
5	FPR_LED_3	14
3	FPR_LED_4	15
1	FPR DET(GND)	16

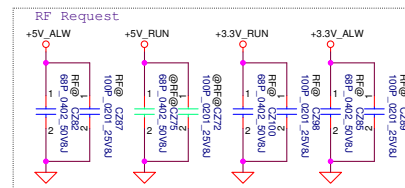
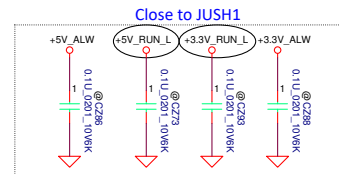
ESD Request



USH CONN



Use HRS_TP31C-26S-01-SM-800 footprint



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USH & TPM & FP	
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Reserve HDD/ODD/FFS Conn	
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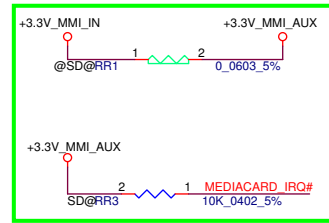
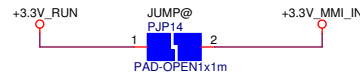
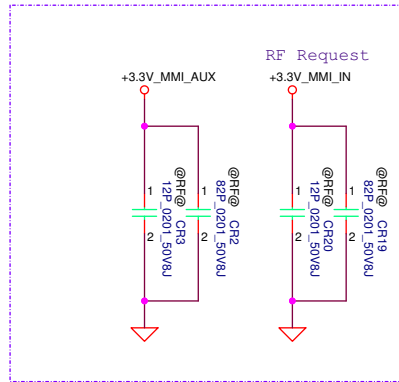


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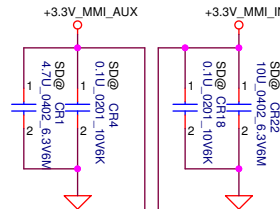
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Title			
eMMC/UFS			
Size	Document Number		Rev
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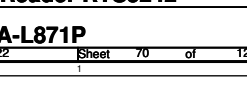
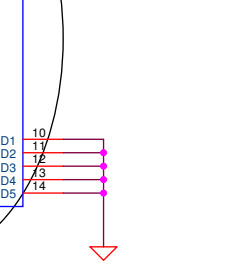
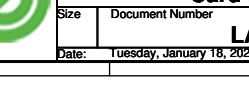
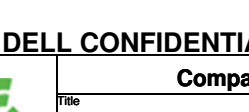
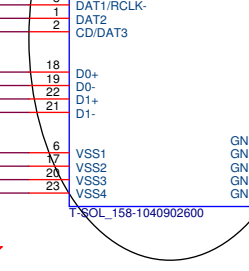
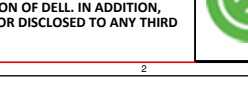
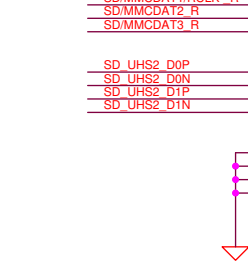
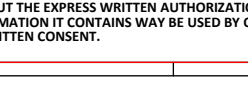
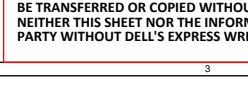
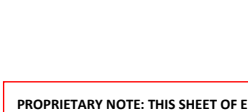
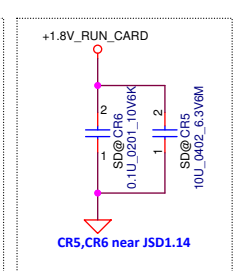
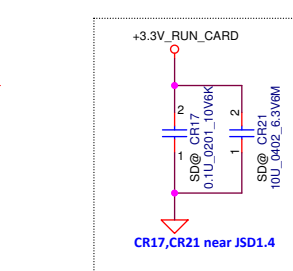
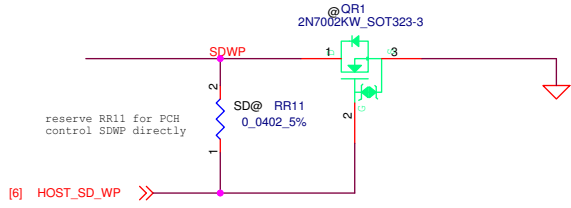
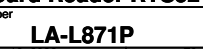
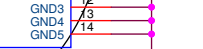
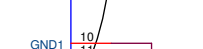
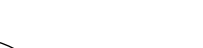
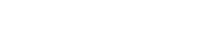
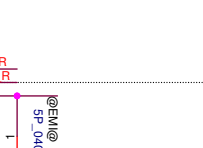
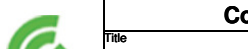
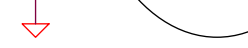
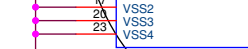
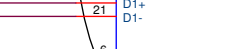
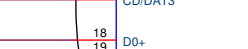
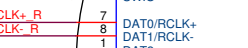
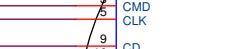
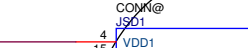
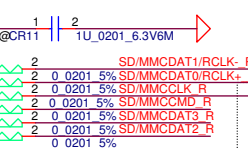
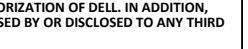
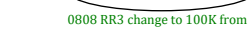
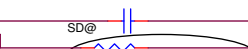
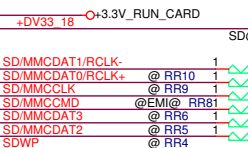
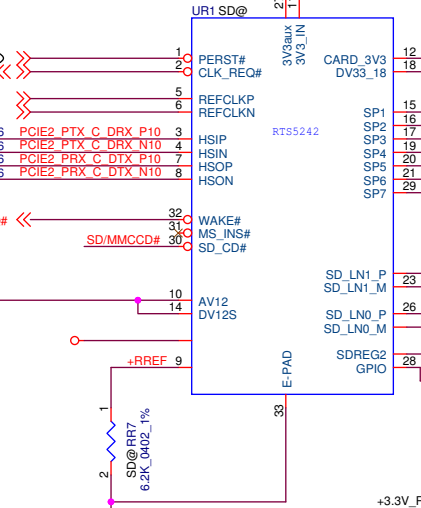
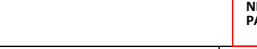
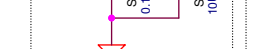
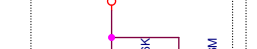
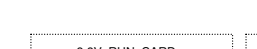
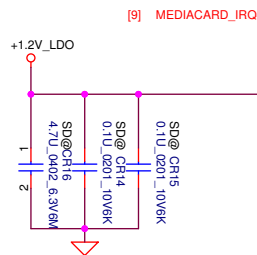
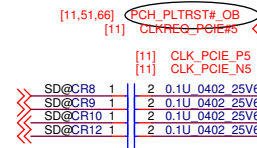
For PCIE Interface



Support D3 Hot(if support D3 cold need control PIN11 3V3_MMI_IN on/off)



- [12] PCIE2_PTX_DRX_P10
- [12] PCIE2_PTX_DRX_N10
- [12] PCIE2_PRX_DTX_P10
- [12] PCIE2_PRX_DTX_N10



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Card Reader RTS5242

LA-L871P

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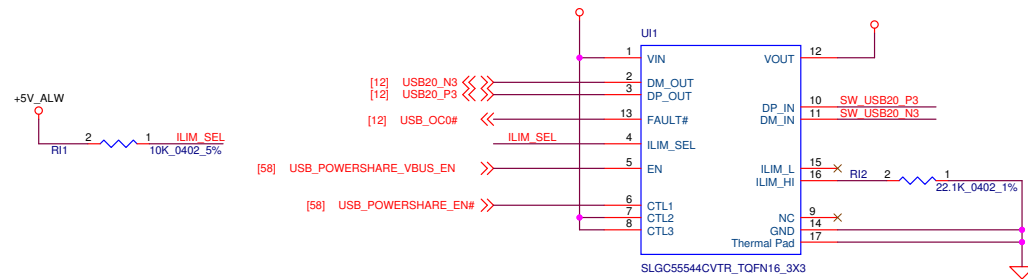
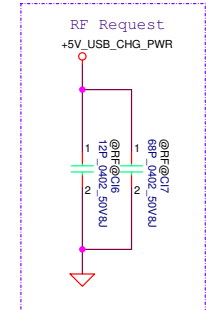
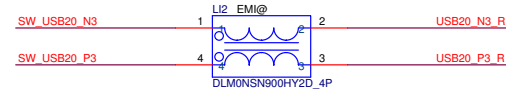
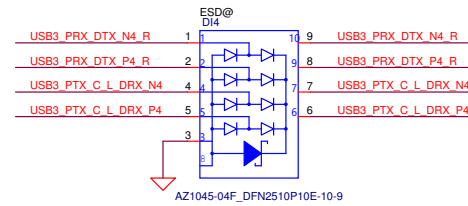
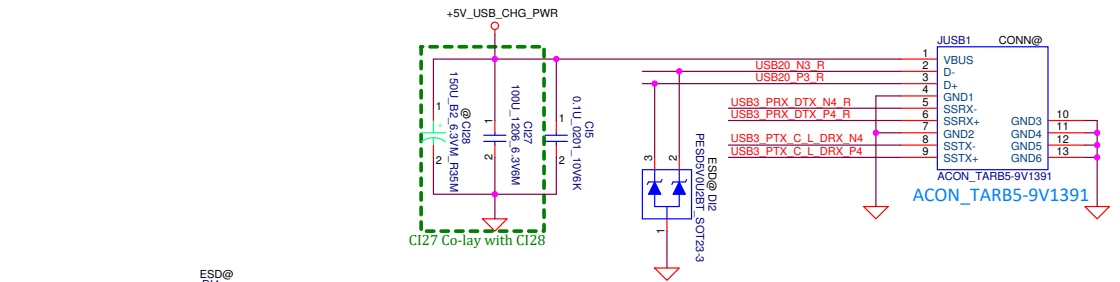


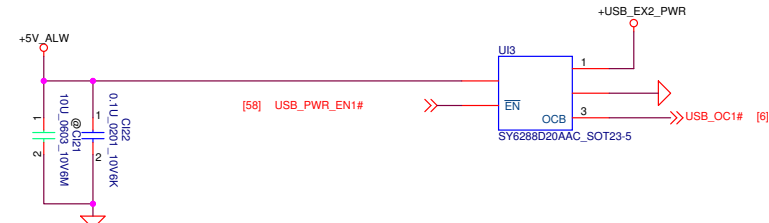
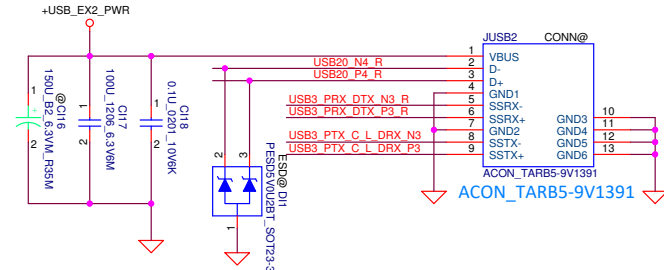
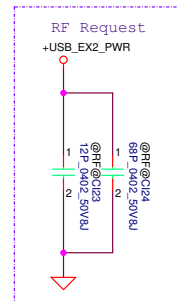
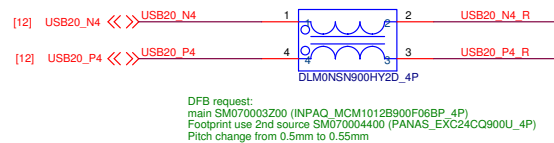
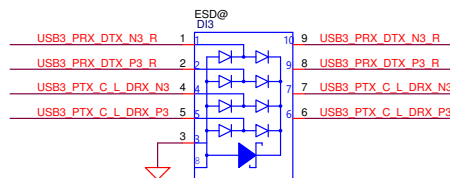
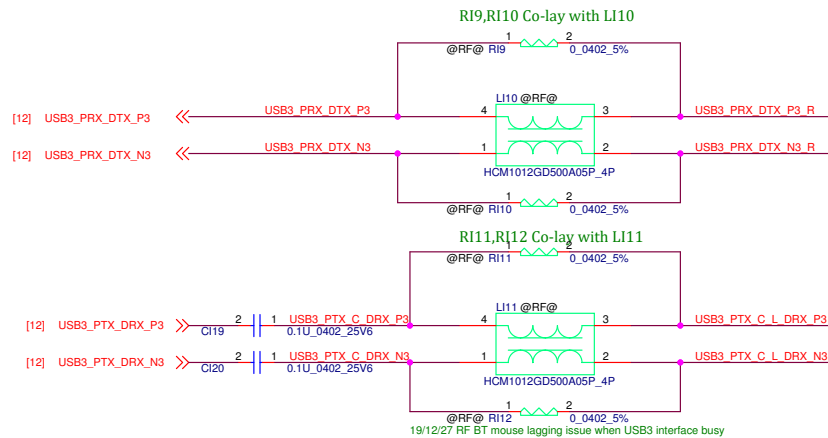
Diagram of a 5V ALW regulator circuit. The input is +5V ALW. The output is connected to a load (represented by a triangle) and a capacitor C14 (0.1uF, 0.0201, 10V6K). The regulator is an RF023 (100P, 0.0201, 50V6J). The feedback network consists of two capacitors: C13 (47uF, 0.023, 6.3V6M) and C11 (47uF, 0.023, 6.3V6M). The output is labeled "Place near UI3.1".

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JUSB1+PS			
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JUSB2		
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Title		
USB2/USB3 DB		
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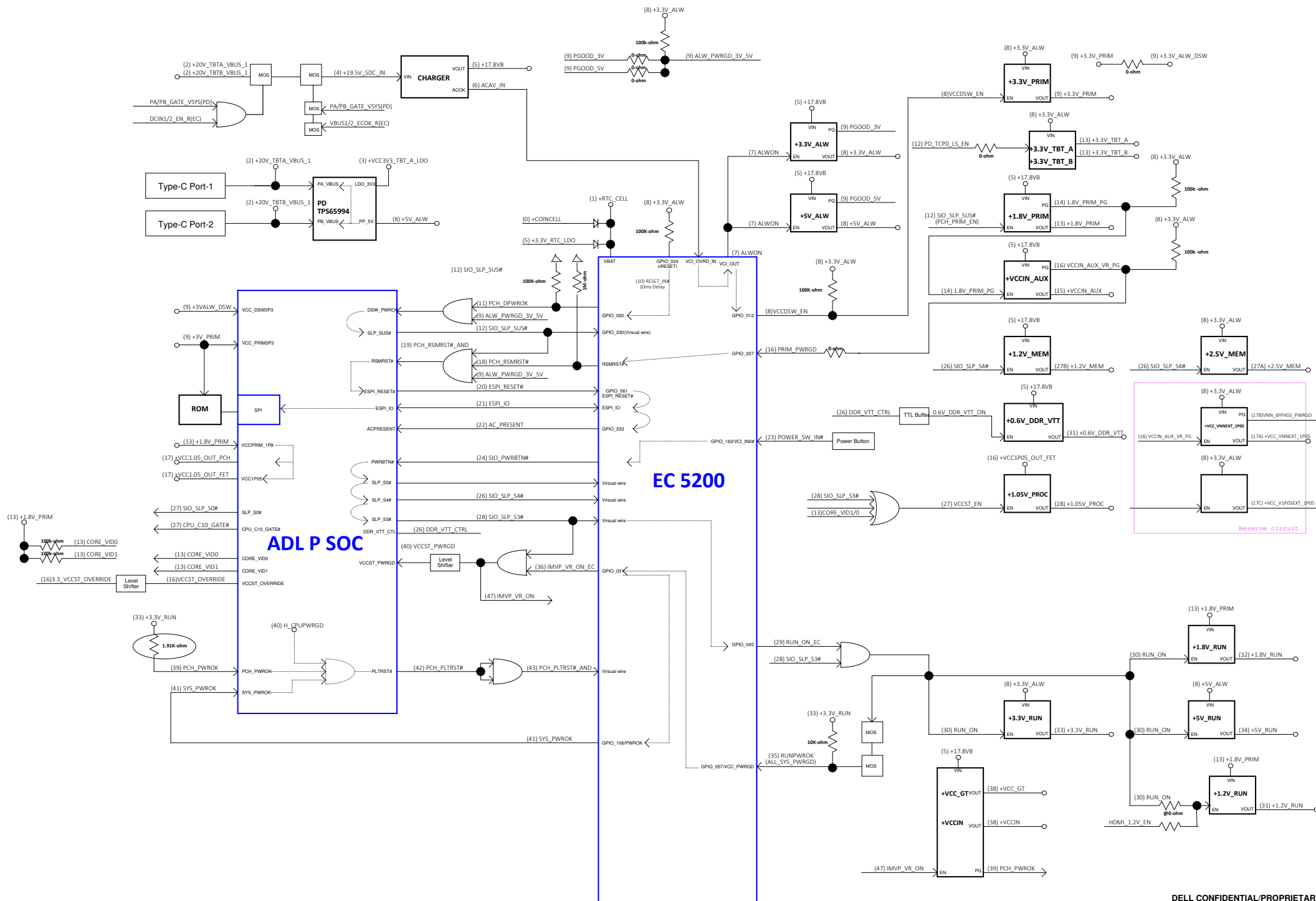
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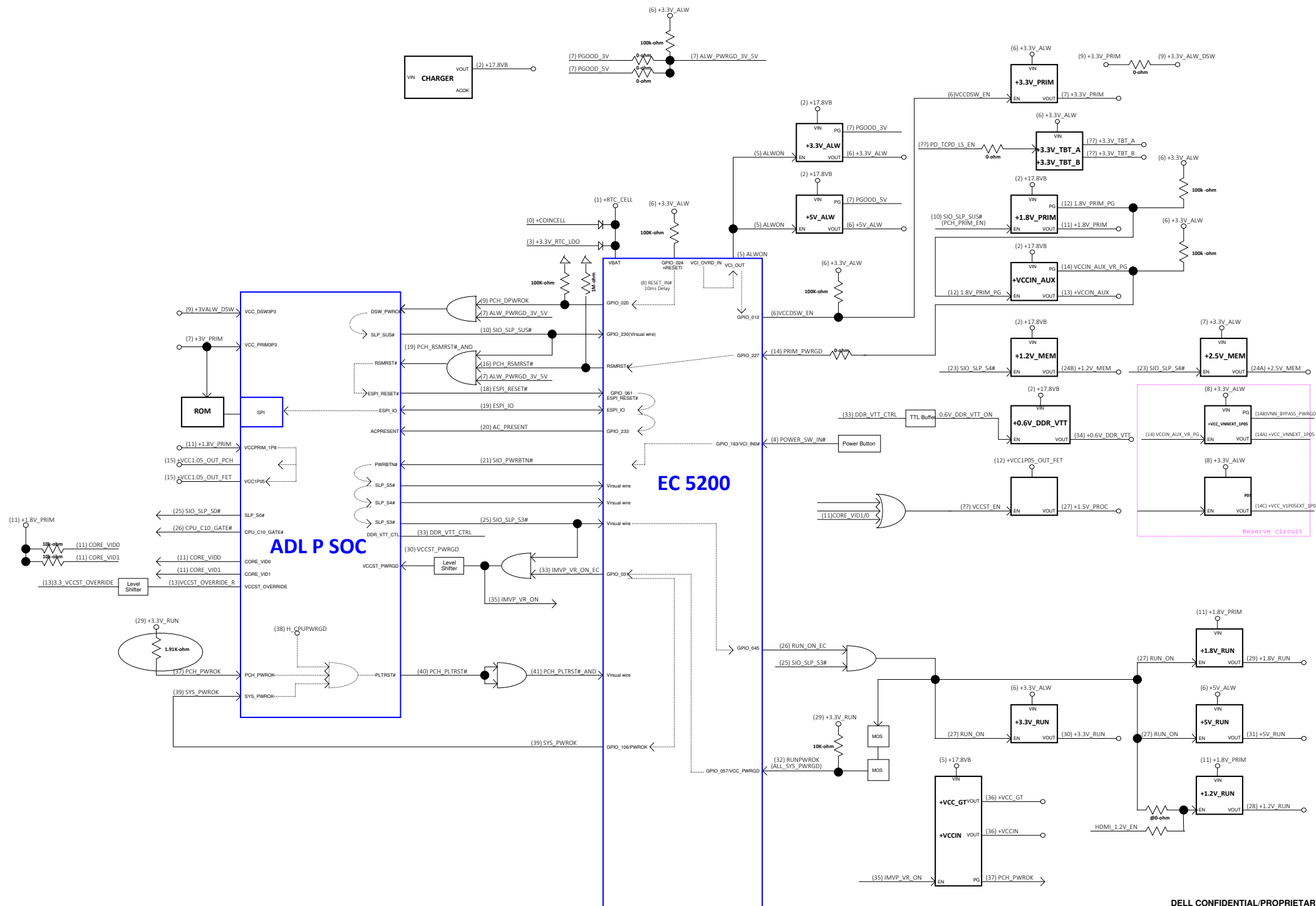
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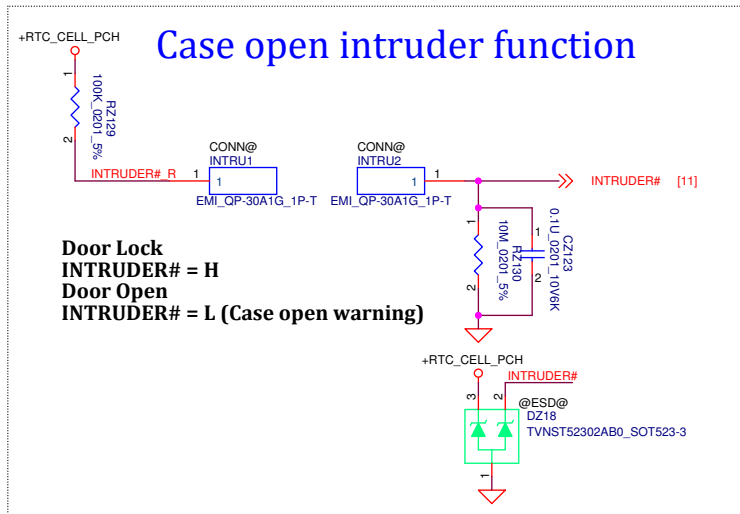
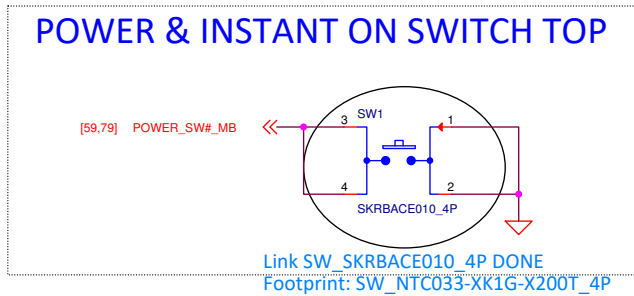
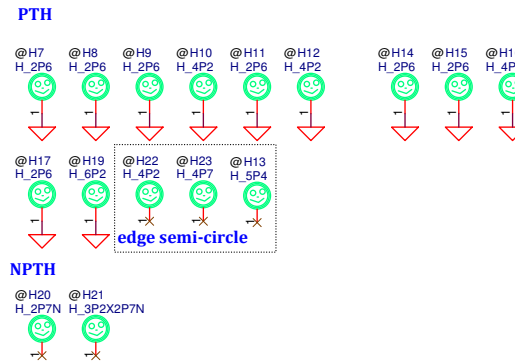
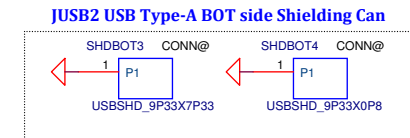
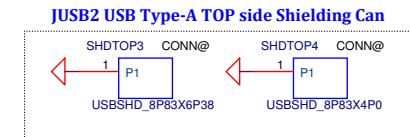
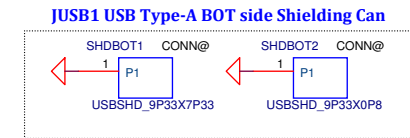
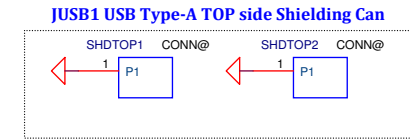
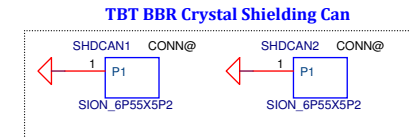
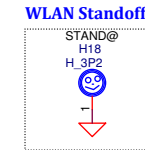
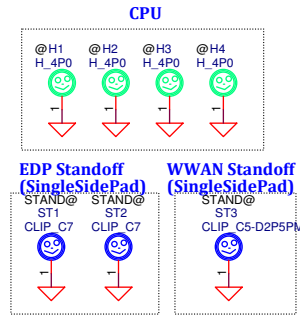
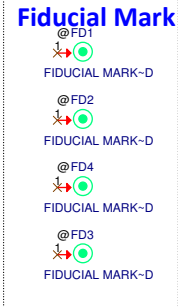
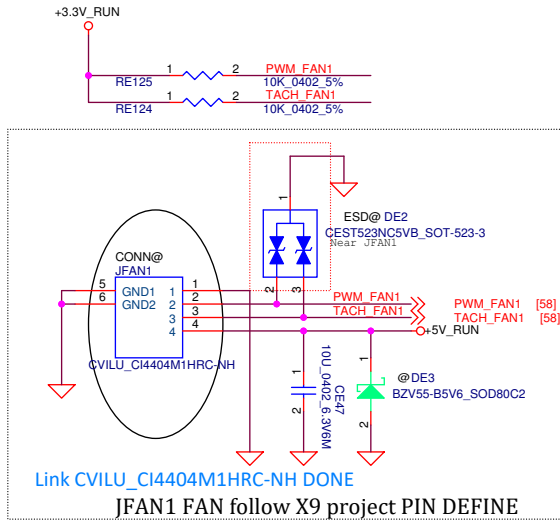
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Size	Document Number		Rev
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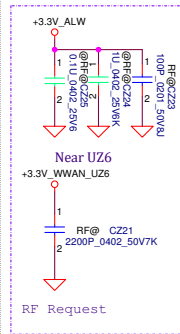
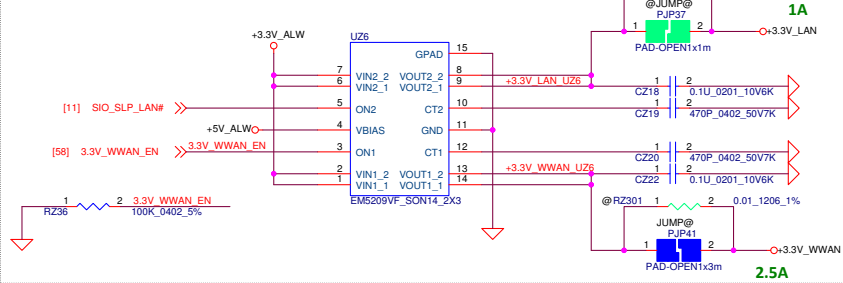
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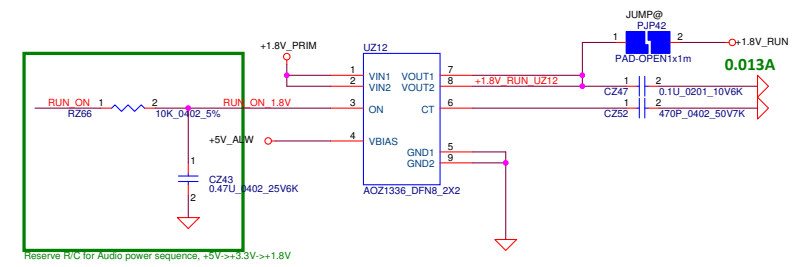
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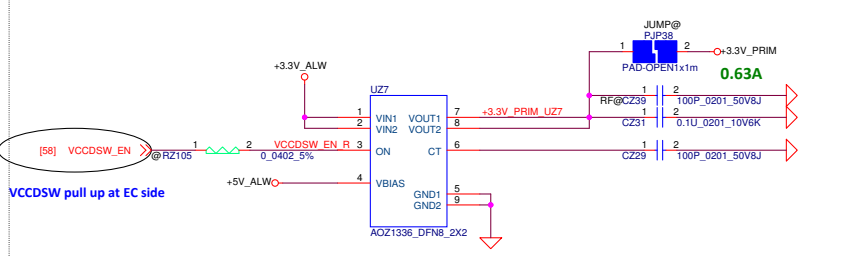
+3.3V_LAN/+3.3V_WWAN source



+1.8V_RUN source

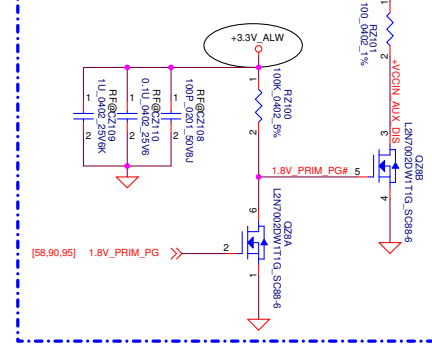


+3.3V_PRIM

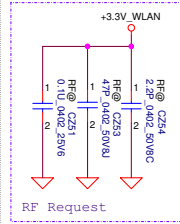
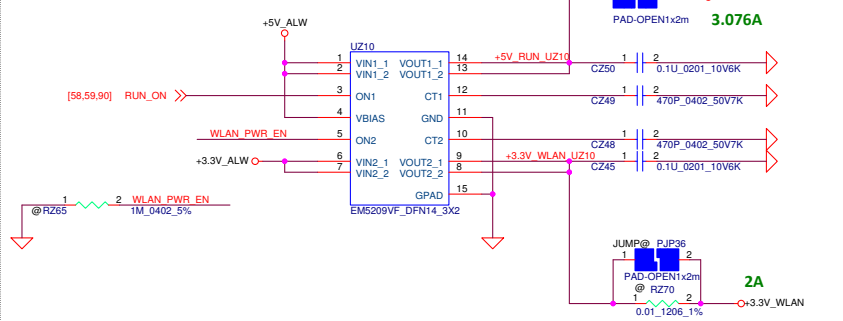


+VCCIN_AUX discharge circuit

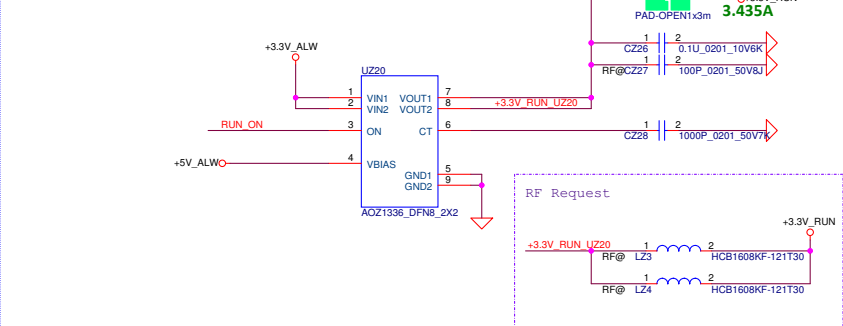
Need to be close to the source(PL501)



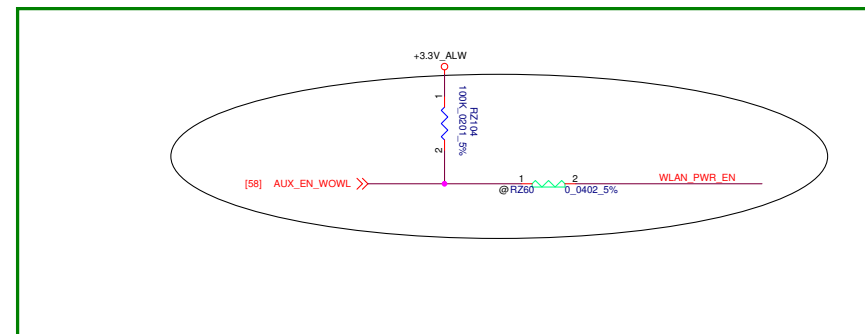
+5V_RUN/+3.3V_WLAN source



+3.3V_RUN source



EC request to reserve OR gate for WLAN power enable



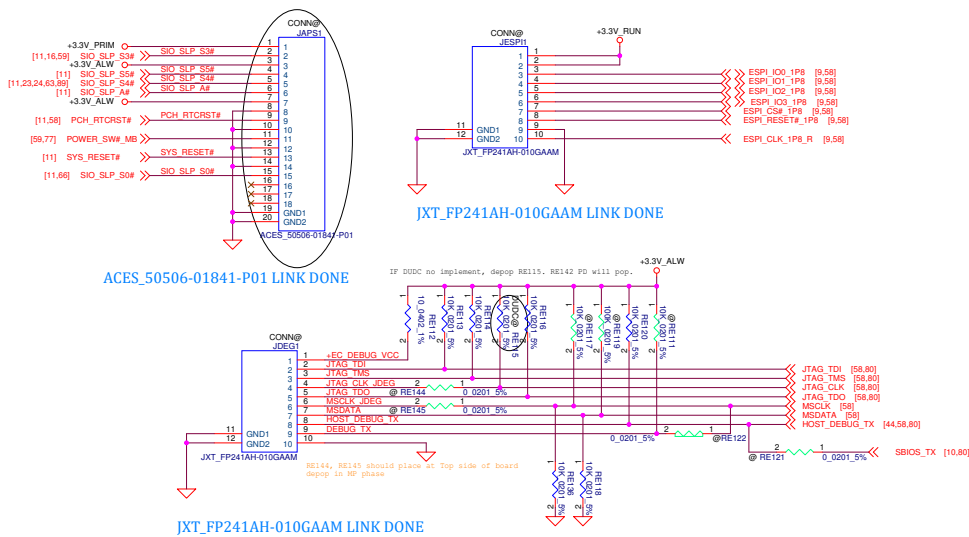
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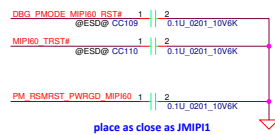


Power control		Rev
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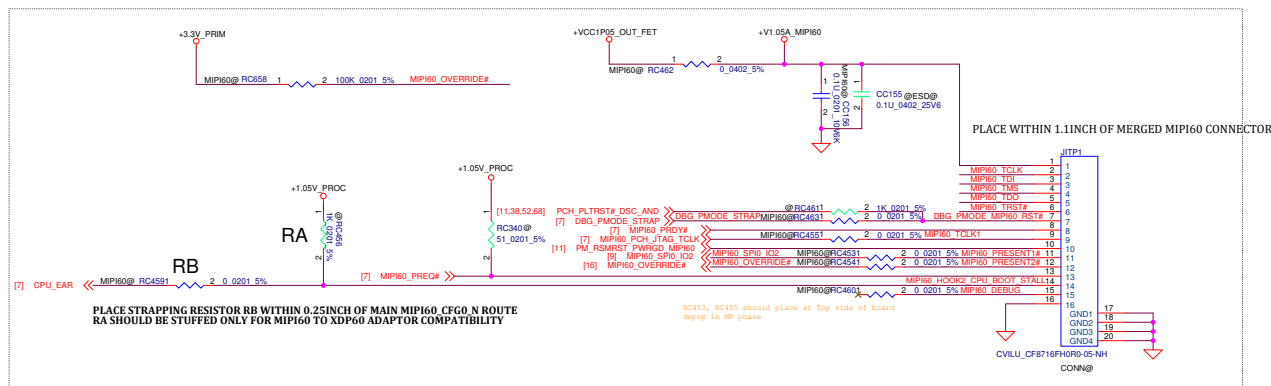
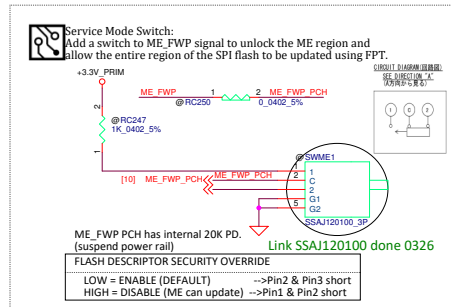
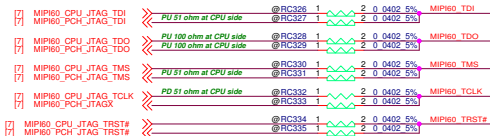
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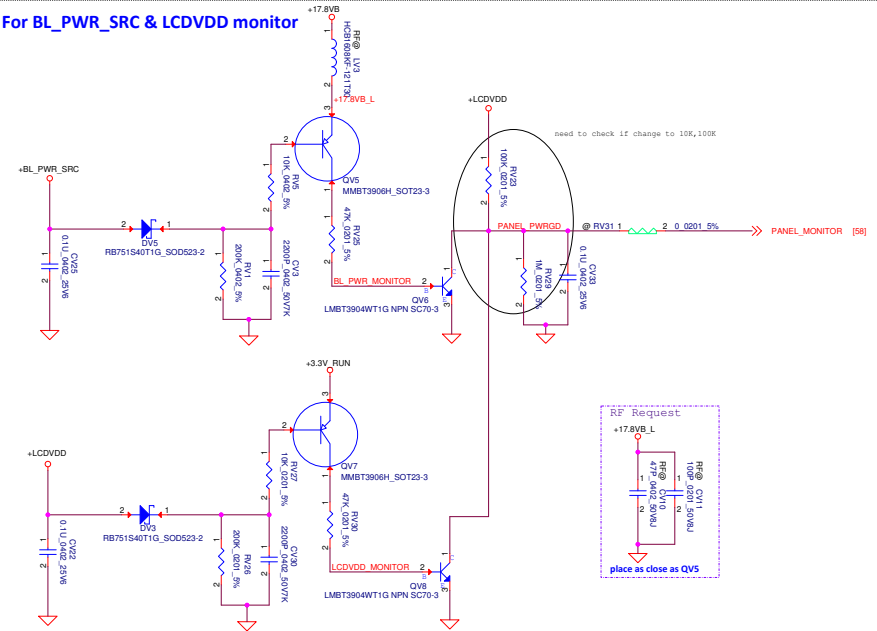
ESD request



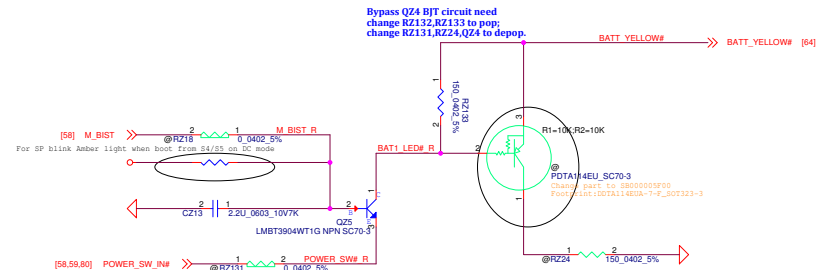
PLACE WITHIN 1.1INCH OF MERGED MIP160 CONNECTOR



For BL_PWR_SRC & LCDVDD monitor



M-BIST



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MIP60/CMC/APS...debug

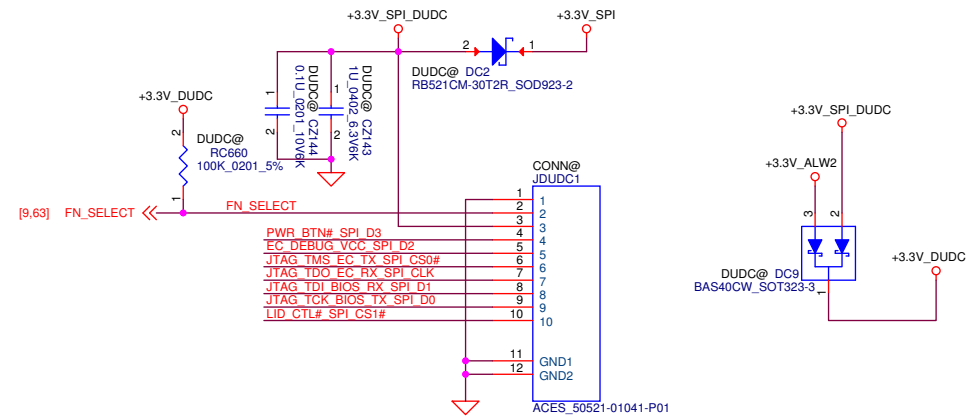
LA-L871P

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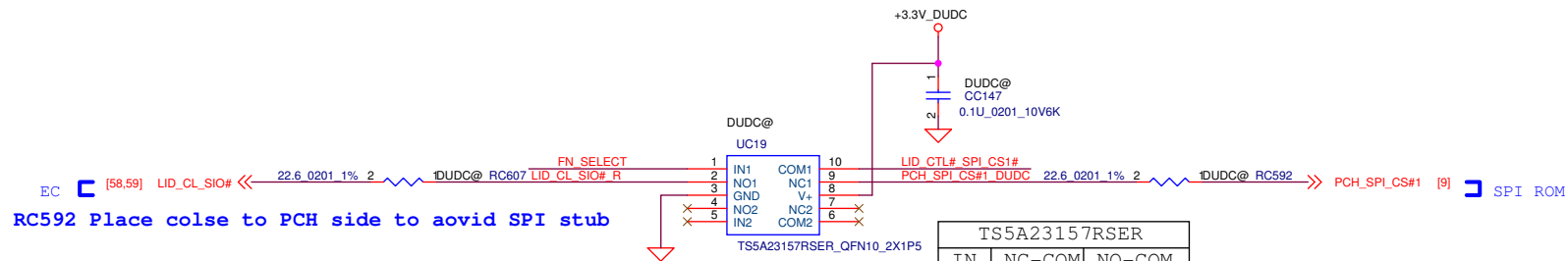
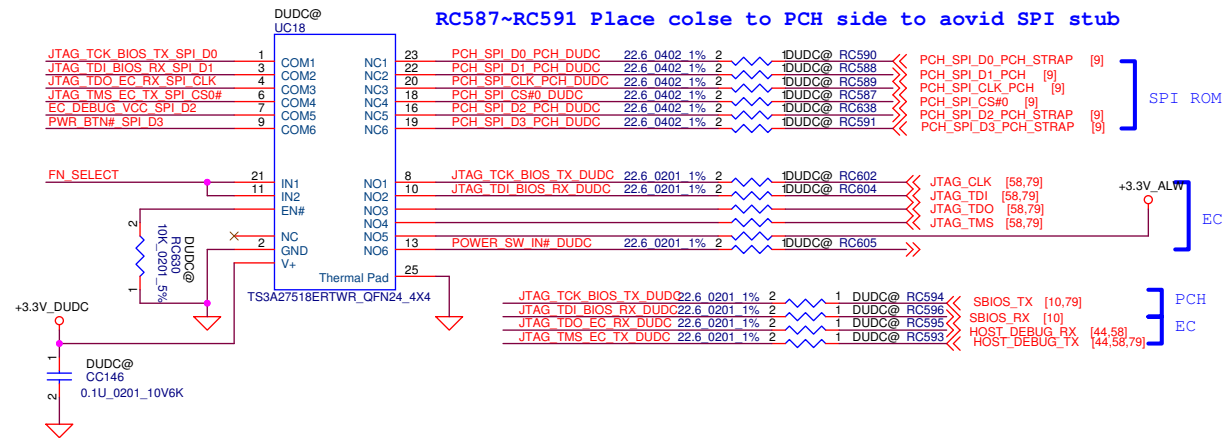
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DUDC Function Table

Pin	Pin Name	Function0 (SPI)	Function1 (Debug)
1	GND	GND	GND
2	FN_SELECT	FN_SELECT=0	FN_SELECT=1
3	+3.3V_SPI_DUDC	+3.3V_SPI_DUDC	+3.3V_SPI_DUDC
4	PWR_BTN#_SPI_D3	PCH_SPI_D3_PCH	POWER_SW_IN#
5	EC_DEBUG_VCC_SPI_D2	PCH_SPI_D2_PCH	+3.3V_ALW
6	JTAG_TMS_EC_TX_SPI_CS0#	PCH_SPI_CS#0	JTAG_TMS/HOST_DEBUG_TX
7	JTAG_TDO_EC_RX_SPI_CLK	PCH_SPI_CLK_PCH	JTAG_TDO/HOST_DEBUG_RX
8	JTAG_TDI_BIOS_RX_SPI_D1	PCH_SPI_D1_PCH	JTAG_TDI/SBIOS_RX (PCH)
9	JTAG_TCK_BIOS_TX_SPI_D0	PCH_SPI_D0_PCH	JTAG_CLK/SBIOS_TX (PCH)
10	LID_CTL#_SPI_CS1#	PCH_SPI_CS#1	LID_CL_SIO#



TS3A27518ERTWR						
EN#	IN1	IN2	NC1/2/3- COM1/2/3	NC4/5/6- COM4/5/6	NO1/2/3- COM1/2/3	NO4/5/6- COM4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L				
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON



TS5A23157RSER		
IN	NC-COM	NO-COM
L	ON	OFF
H	OFF	ON

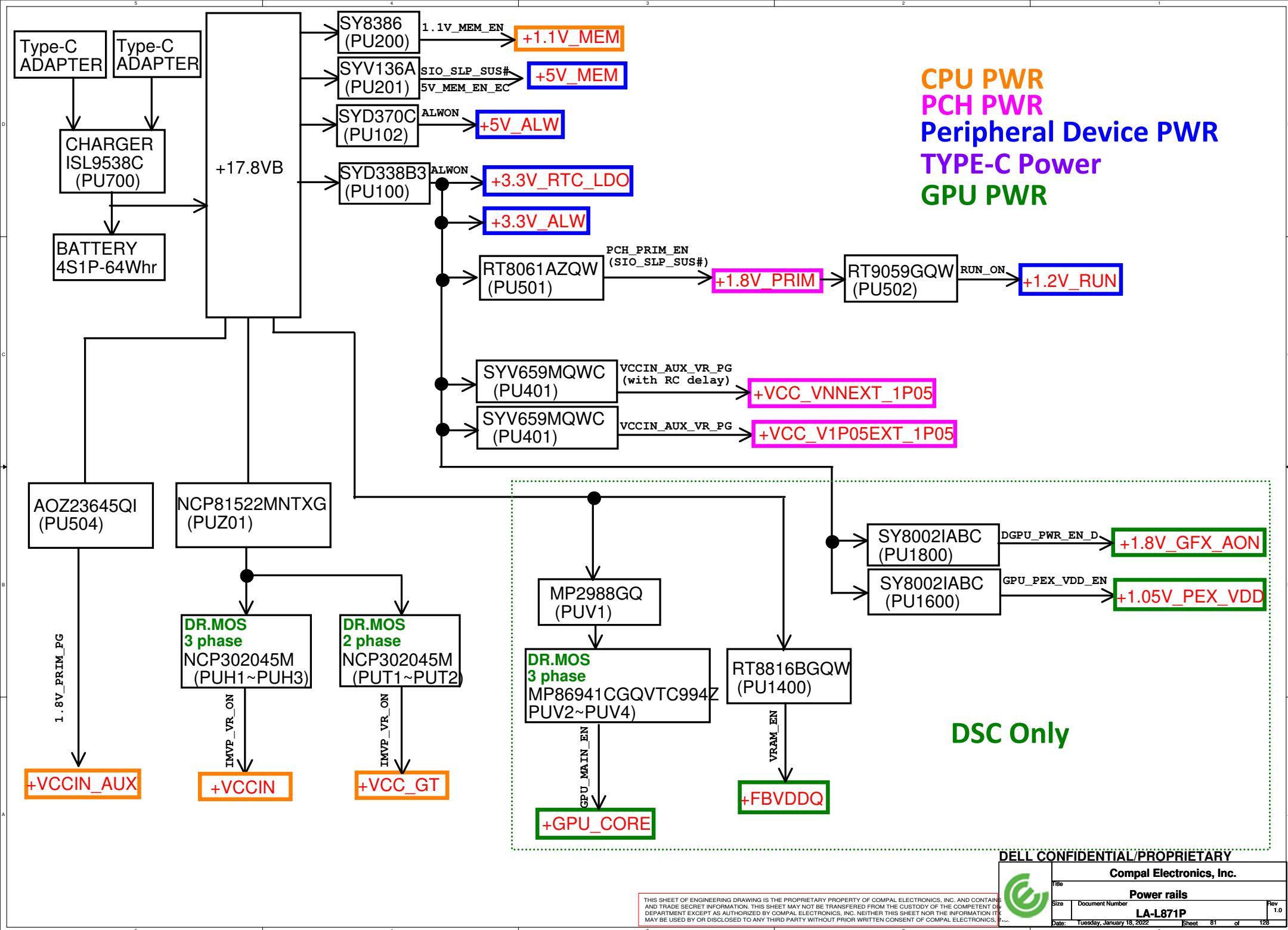
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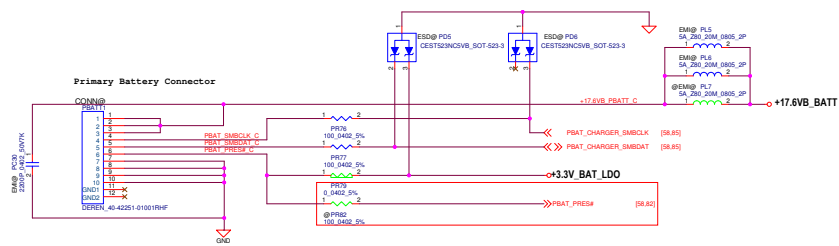


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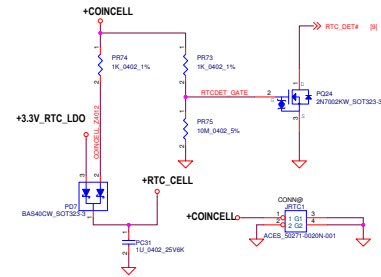
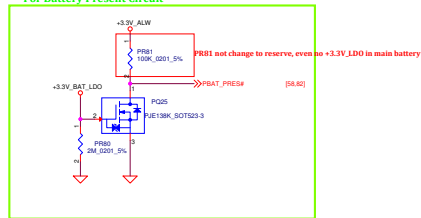
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DUDC		
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For Battery Present Circuit



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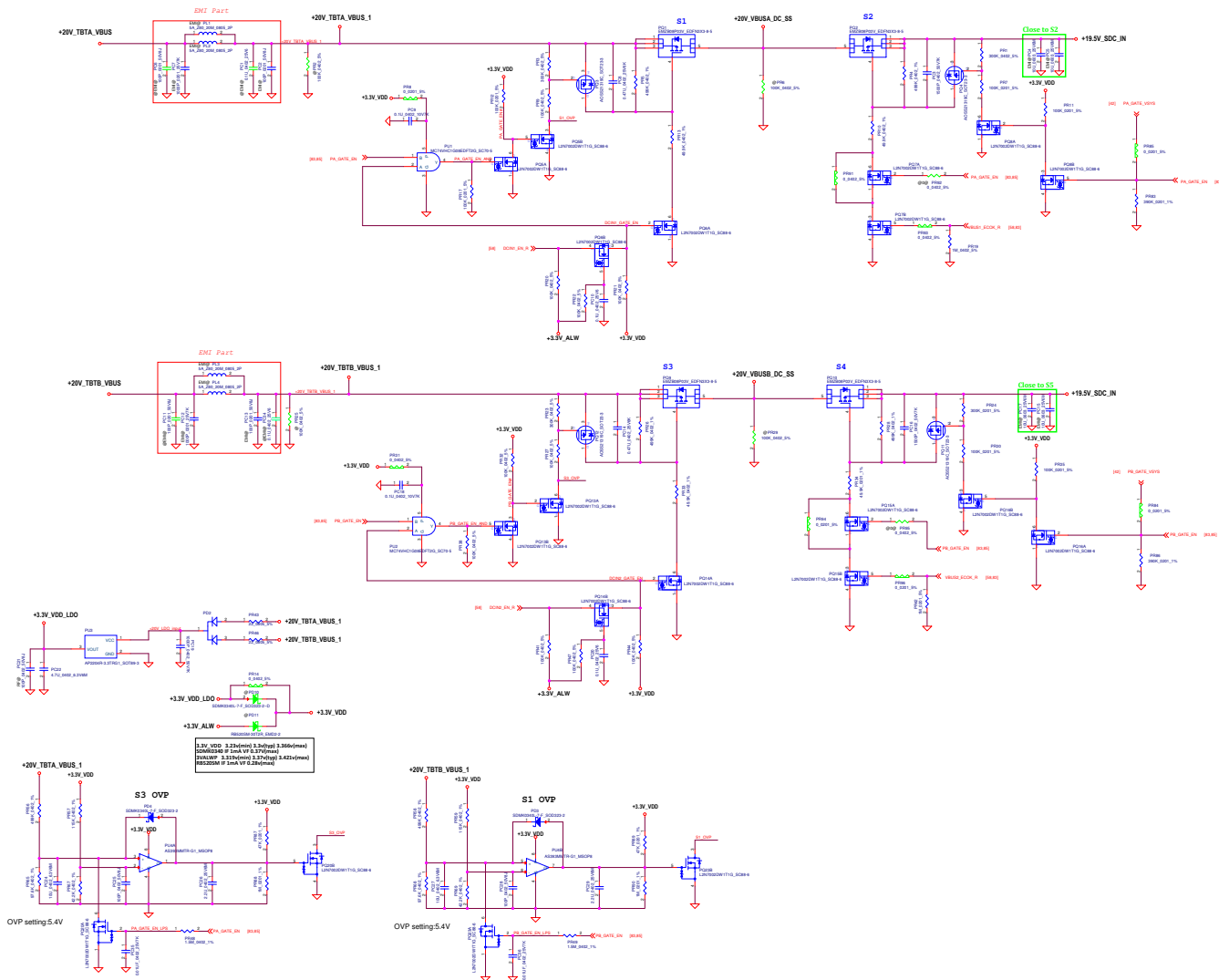
Compel Electronics, Inc.

Battery Connector/ RTC

LA-L871P


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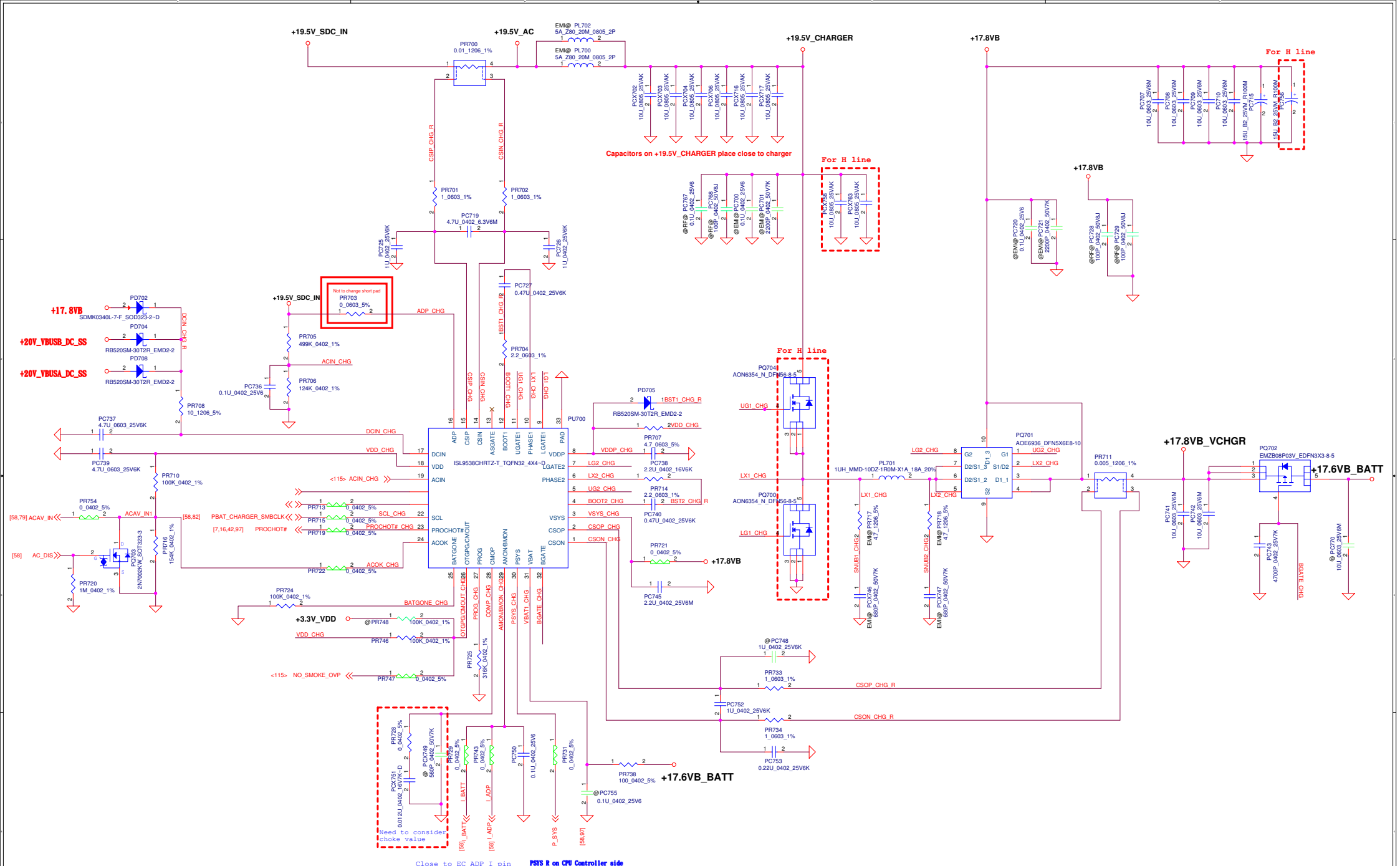


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Close to EC ADP_i pin PSYS R on CPU Controller side

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Charger


LA-L871P

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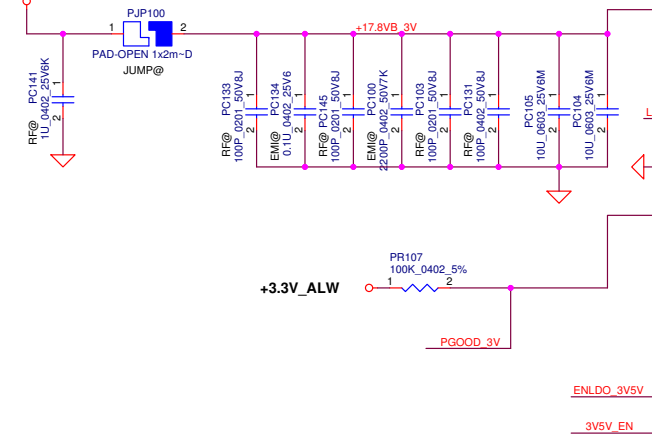
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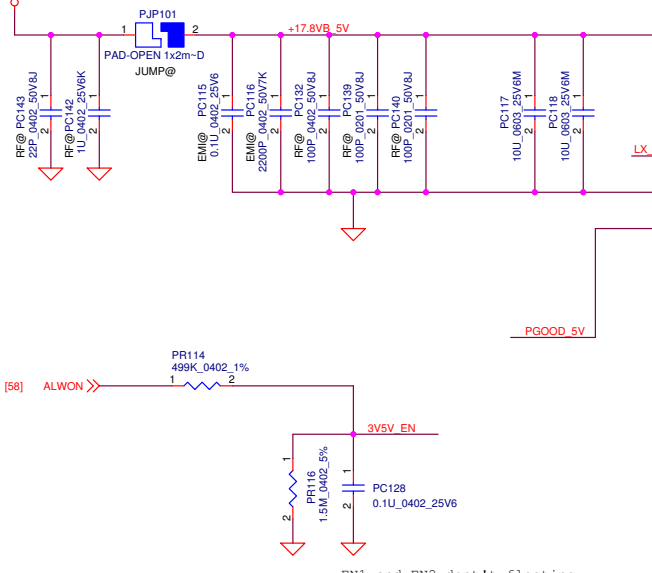
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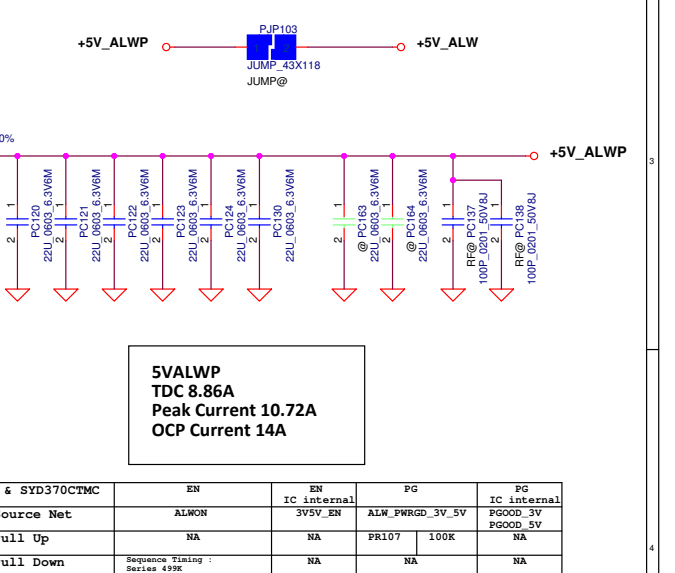
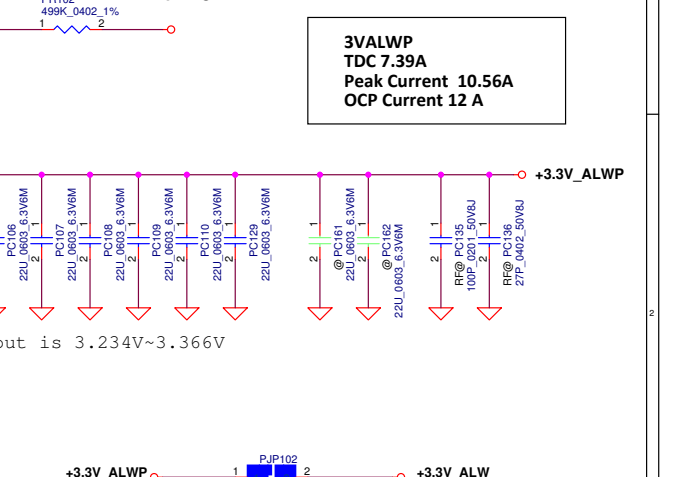
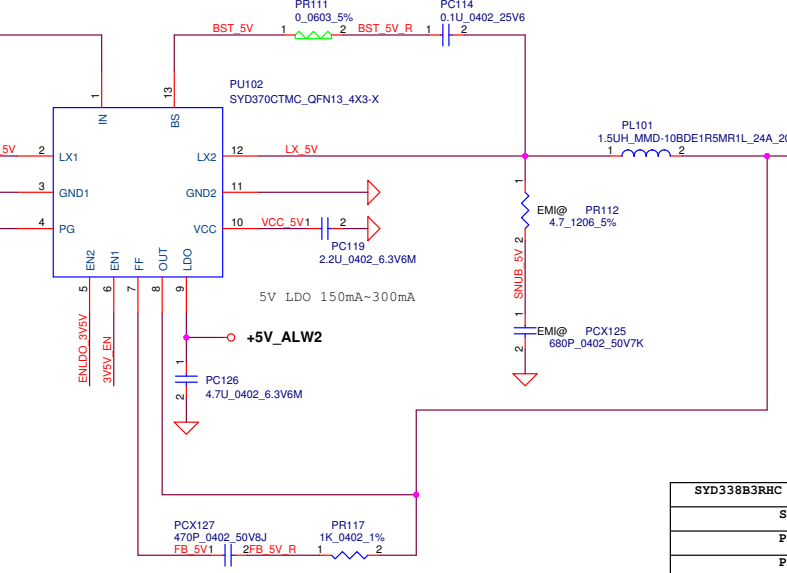
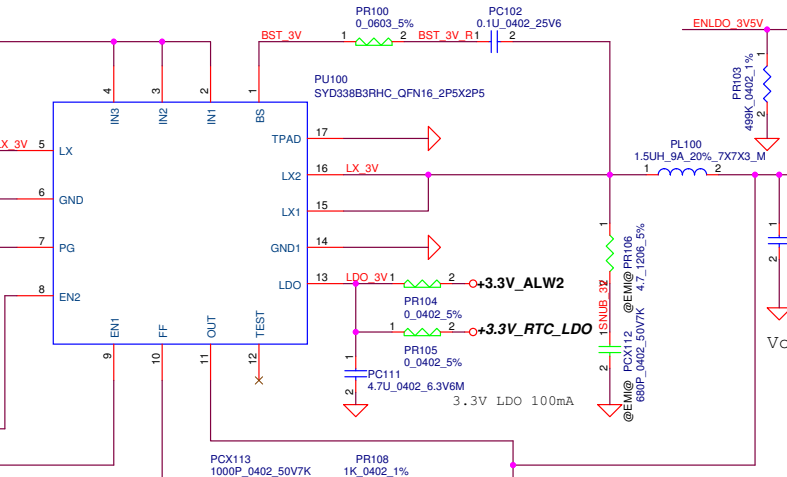
+17.8VB



+17.8VB



EN1 and EN2 don't floating



3VALWP
TDC 7.39A
Peak Current 10.56A
OCP Current 12 A

5VALWP
TDC 8.86A
Peak Current 10.72A
OCP Current 14A

	EN	EN	PG	PG
	IC internal	IC internal	ALW_PWRGD_3V_5V	PGOOD_3V
Source Net	ALWON	3V5V_EN	ALW_PWRGD_3V_5V	PGOOD_3V
Pull Up	NA	NA	100K	NA
Pull Down	NA	NA	NA	NA


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+5V_ALW/3.3V_ALW	
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+17.8VB

PAD-OPEN1x1m
JUMP@

RF demand

+17.8VB 1.1VDDR

LX 1.1VDDR

+3.3V_ALW

+1.1V_DDRP

+1.1V_MEM

+1.1V_DDRP

+1.1V_MEM

+1.1V_DDRP

[58.78.95] 1.1V_MEM_PWRGD <<

For DDR 5V OVP

[58.78.95] SIO_SLP_S4# <<

[11] 1.1V_MEM_EN >>

ILMT setting	Current Limit
Low	6A
Floating	8A
High	10A

The current limit is set to 6A , 8A or 10A when this pin is pull low, floating or pull high

+17.8VB

+17.8VB_5VDDR

+3.3V_ALW

LX 5VDDR

+3.3V_ALW

+5V_DDRP

+5V_MEM

+5V_DDRP

+5V_MEM

+5V_DDRP

For DDR 5V OVP

+3.3V_ALW

MODE_5VDDR

LIMIT_5VDDR

+3.3V_ALW

+5V_DDRP

+5V_MEM

+5V_DDRP

+5V_MEM

+5V_DDRP

MODE	SIO_SLP_S4#	MODE_5VDDR
FCM	L	H
PFM	H	L


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+1.1V MEM/+5V DDR	
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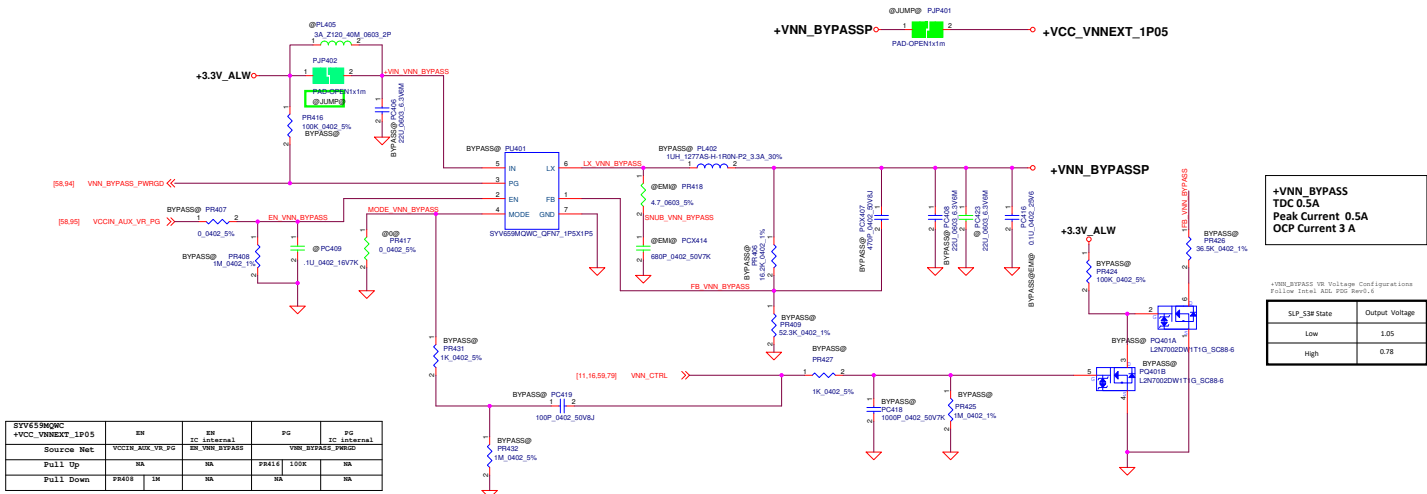
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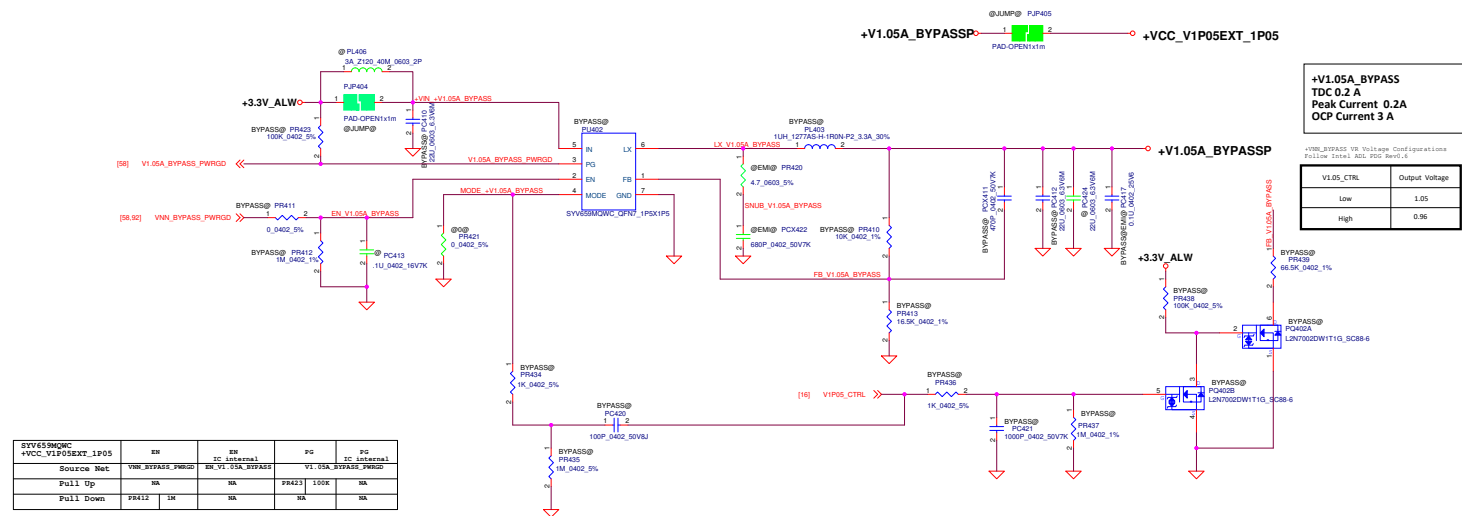
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VCC_VNNEXT_1P05 (VNN_BYP) and VCC_V1P05EXT_1P05 (V1P05_BYP) are two dedicated voltage regulators that save platform power during low power states (Sx/S0ix). Both VCC_V1P05EXT_1P05 and VCC_VNNEXT_1P05 are VIded rails that operate at two voltage levels each. The VId control for this VR is the SLP_S3# signal.



VCC_VNNEXT_1P05 (VNN_BYP) and VCC_V1P05EXT_1P05 (V1P05_BYP) are two dedicated voltage regulators that save platform power during low power states (Sx/S0ix). Both VCC_V1P05EXT_1P05 and VCC_VNNEXT_1P05 are VIded rails that operate at two voltage levels each. The VId control for this VR is the SLP_S3# signal.

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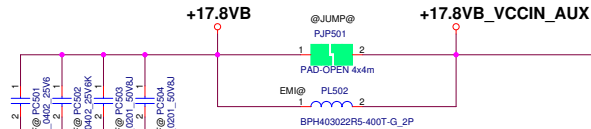
Compal Electronics, Inc.

+VNN V1.05A_BYPASS

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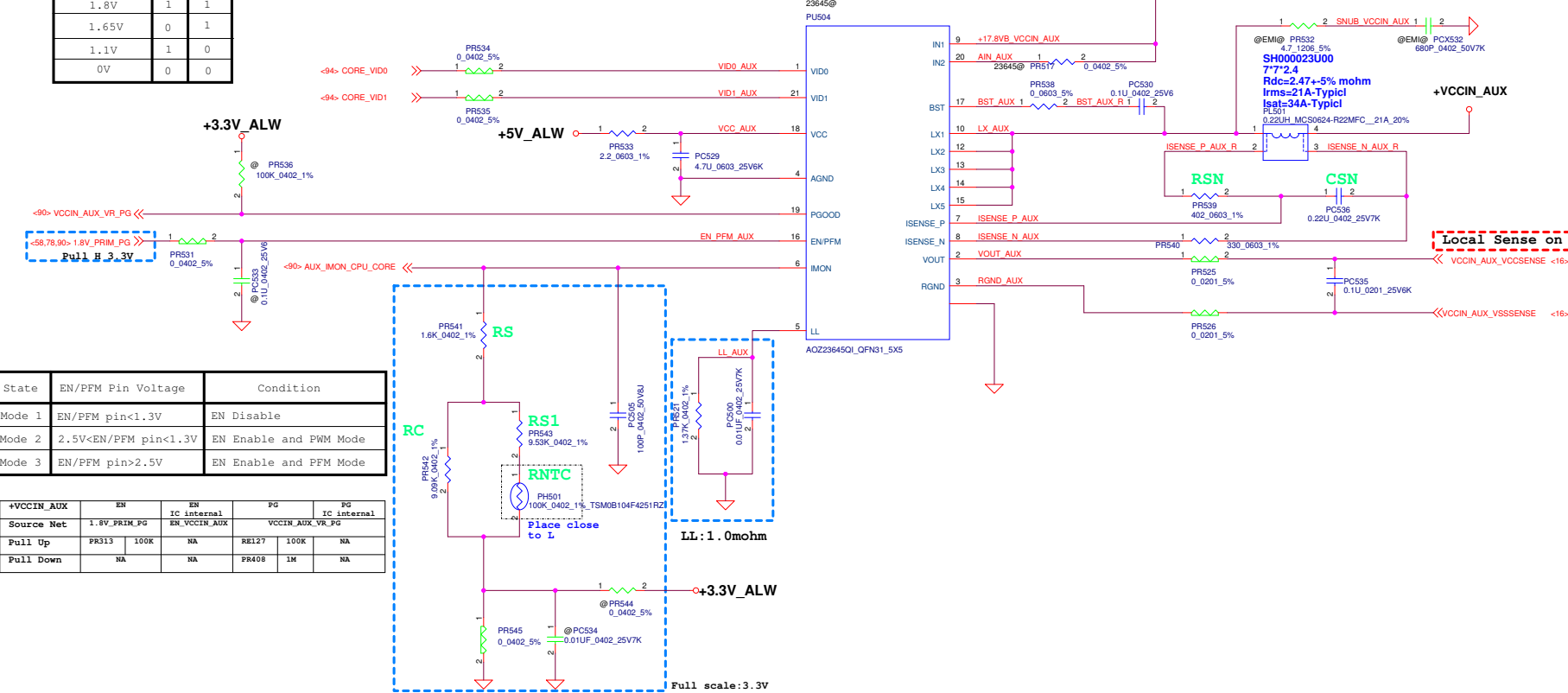
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Output Voltage for Corresponding VID Setting

VOUT Setting	VID0	VID1
1.8V	1	1
1.65V	0	1
1.1V	1	0
0V	0	0



+VCCIN_AUX
TDC :14A
Peak Current 32A (ICCmax)
Valley Current limit :32A(min) by IC pin.14 setting
DC Load line :NA
AC Load line :NA
Fsw=800kHz

State	EN/PFM Pin Voltage	Condition
Mode 1	EN/PFM pin<1.3V	EN Disable
Mode 2	2.5V<EN/PFM pin<1.3V	EN Enable and PWM Mode
Mode 3	EN/PFM pin>2.5V	EN Enable and PFM Mode

+VCCIN_AUX	EN	EN IC internal	PG IC internal
Source Net	1.8V_PRIM_PG	EN_VCCIN_AUX	VCCIN_AUX_VR_PG
Pull Up	PR313 100K	NA	RE127 100K
Pull Down	NA	NA	PR408 1M

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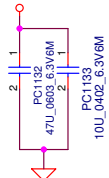
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+VCCIN_AUX	
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AUX Decoupling Cap

+VCCIN_AUX_FILTR

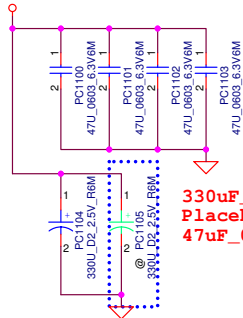
+VCCIN_AUX



47uF_0603 *1 pcs
Placeholder_0402 *1pcs

Primary Side

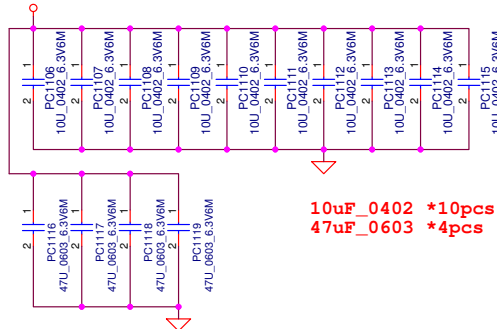
+VCCIN_AUX



330uF_4.5m_ohm_7343 *1
Placeholder_7343*1
47uF_0603 *4 pcs

Secondary side

+VCCIN_AUX



10uF_0402 *10pcs
47uF_0603 *4pcs

Follow Intel ADL-P PDG Rev1p0 PDF 2021/02/20
+VCCIN_AUX Output CAP :

Primary Side:
330uF_4.5m_ohm_7343 *1 PCS
47uF_0603 *4 pcs

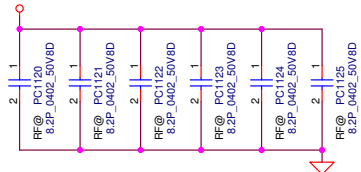
Secondary side:
47uF_0603 *4pcs
10uF_0402 *10pcs

+VCCIN_AUX_FILTR :

Primary Side:
47uF_0603 *1 pcs
Placeholder_0402 *1pcs

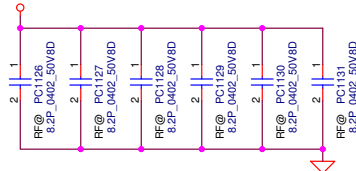
RF Decoupling cap

+VCCIN_AUX



Follow Intel ADL-P PDG Rev0p8 PDF 2020/11/12
RF Decoupling cap *6 for FIVR Input Power Plans

+VCCIN_AUX



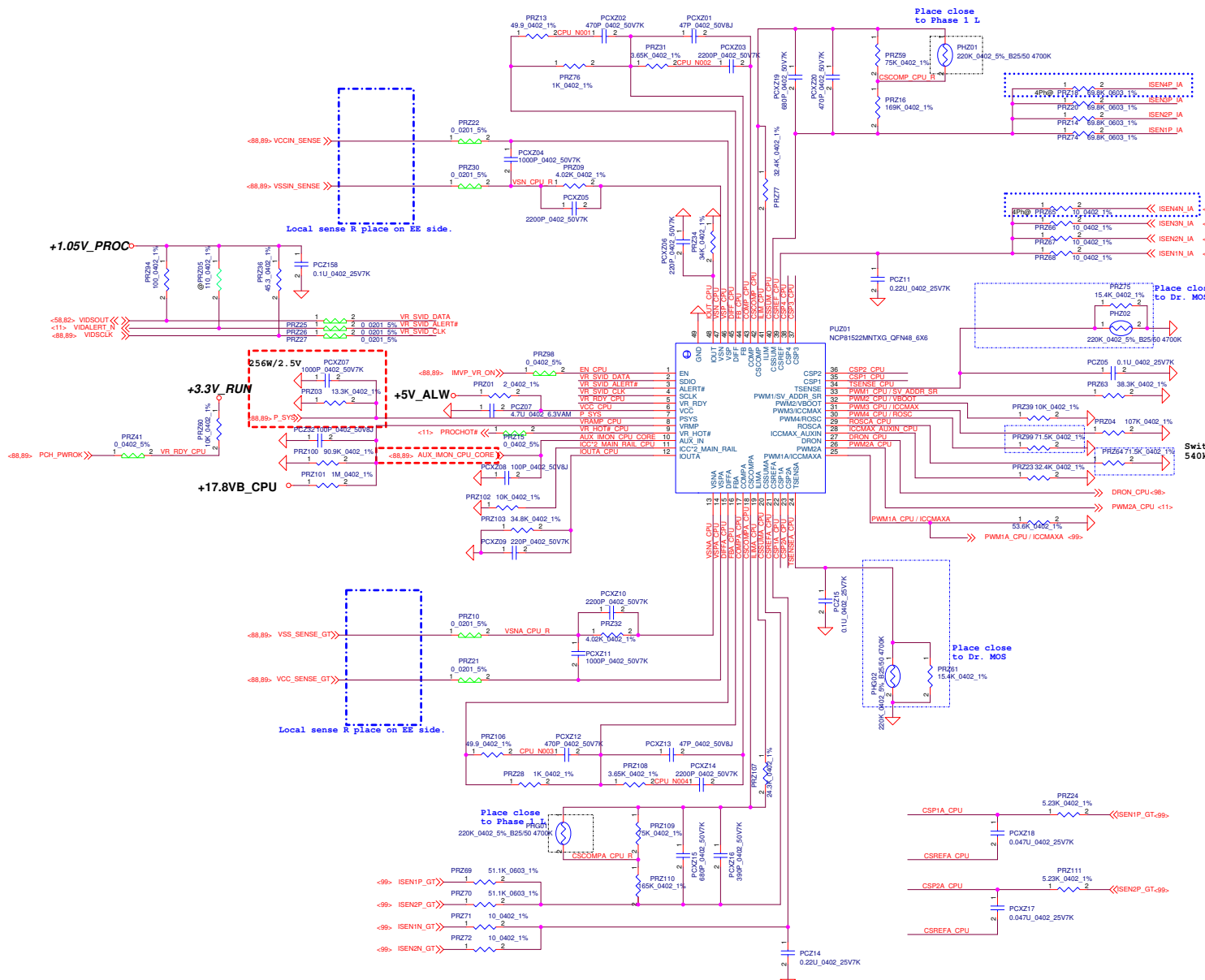
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		VCCIN_AUX Decoupling CAP	
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Main Func = CPU (IA/GT)



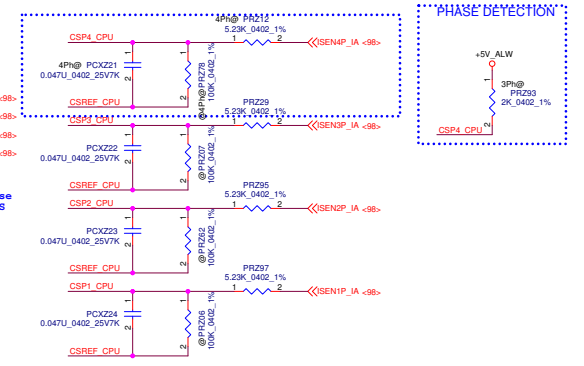
```
Follow Intel PDS ADL-F_V2.0
ADL-F 4+8 28W
Performance:
VCCIN:
ICCMAX=85A      R_DC_LL (mΩ) MAX
Ipl2=50A        VCCON:2.3 mOhm
                 VCCGT:3.2 mOhm

VCCINGT
ICCMAX=55A
Ipl2=30A
```

```
Follow Intel PDS ADL-F_V2.0  
ADL-F 6+8 2W  
Performance:  
VCCIN:  
ICCMAX=109A      R_DC_LL (mΩ) MAX  
Ip12=63A          VCCON:2.3 mOhm  
                  VCCGT:3.2 mOhm  
  
VCCINGT  
ICCMAX=55A  
Ip12=30A
```

SoC Power Levels:
PL1 (TDP) : 28W
PL2 : 64W
PL4 : 90W

SoC Power Levels:
PL1 (TDP) : 28W
PL2 : 64W
PL4 : 140W



Switching Frequency
540kHz

- | | | |
|---|-----------------------|------|
| → | PWM1_CPU / SV_ADDR_SR | <98> |
| → | PWM2_CPU / VBOOT | <98> |
| → | PWM3_CPU / ICCMAX | <98> |
| → | PWM4_CPU / ROSC | <98> |

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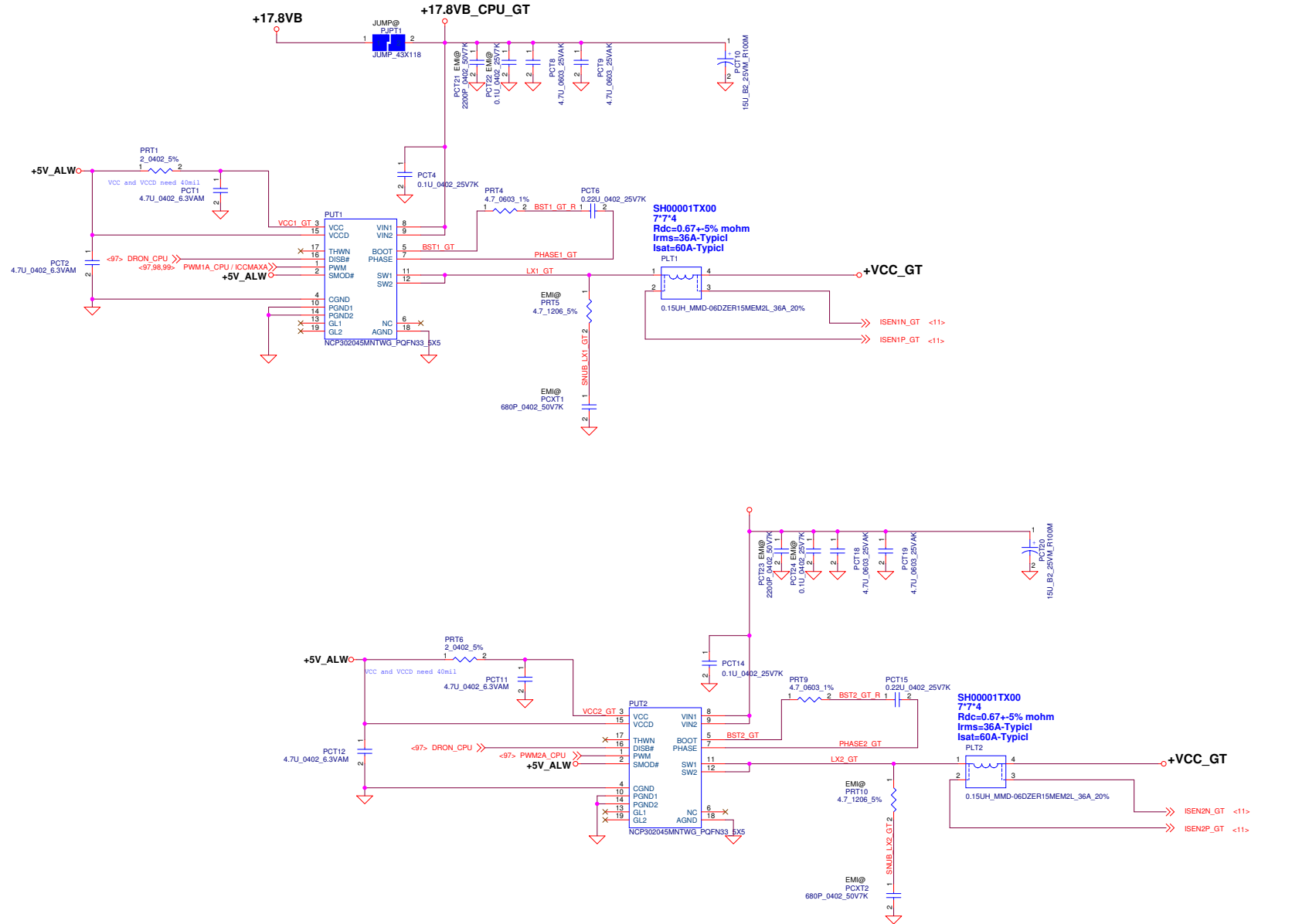
VCCIN_AUX Decoupling CAP

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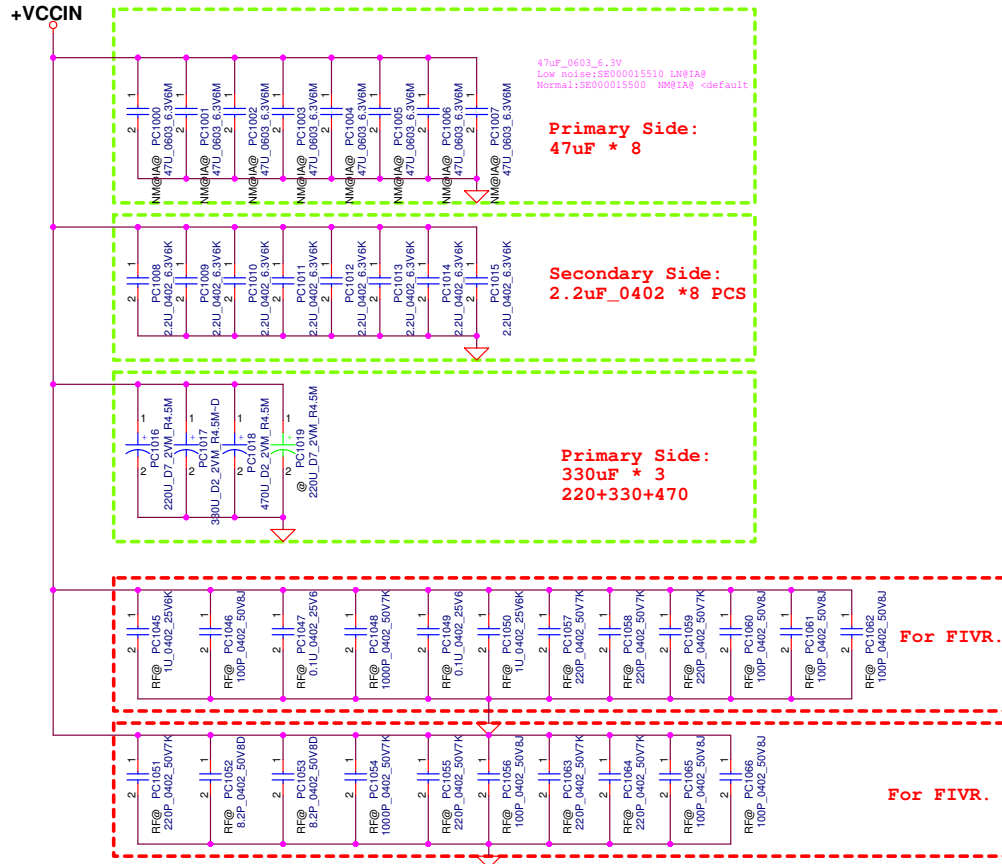
+VCCIN Output CAP :

Primary Side:

330uF 4.5m ohm_7343 *3 PCS
47uF_0603 *8 PCS

Secondary side:

2.2uF_0402 *8 PCS



Follow Intel ADL-P PDG Rev1p0 PDF 2021/02/20

+VCCGT Output CAP :

Primary Side:

330uF 4.5m ohm_7343 *2 PCS
47uF_0603 *7 PCS
Placeholder_0603 *1 PCS
22uF_0603 *2 PCS

Secondary side:

22uF_0603 *6 PCS
10uF_0402*2
Placeholder_0402*1
Placeholder_0603*1

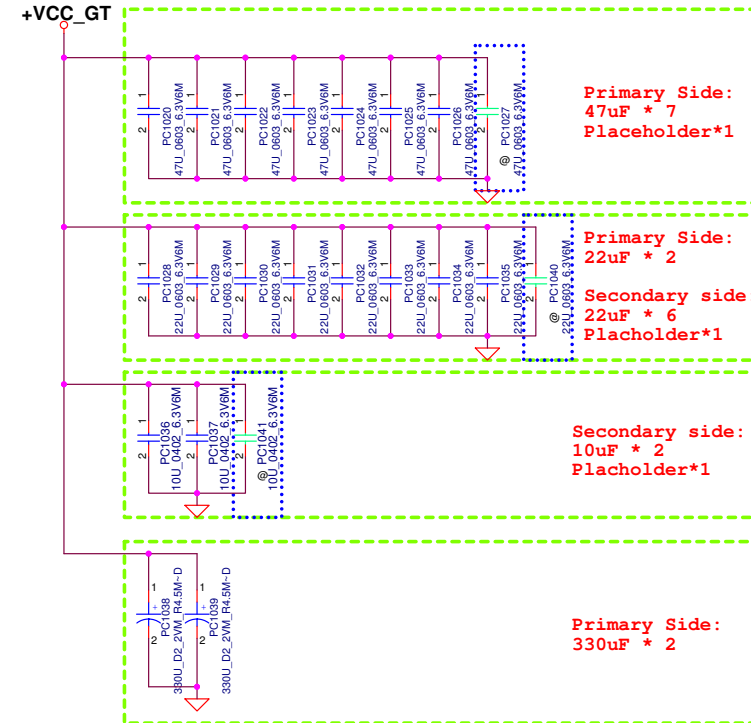


Table 752. Decoupling Solution

Decap Placement	Form Factor	Value	Number	Note	Reference Design
Primary Side	7343	330uF (4.5mOhms ESR)	3	Pair board CAPs with power/ground VIAS. Align CAPs along current flow path from VR to package pins.	VCCCORE_2
Primary Side	0603	47uF	8	Pair board CAPs with power/ground VIAS. Align CAPs along current flow path from VR to package pins.	VCCCORE_2
Secondary side	0402	2.2uF	8	Pair board CAPs with power/ground VIAS. Align CAPs along current flow path from VR to package pins.	VCCCORE_3

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CPU Decoupling			
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
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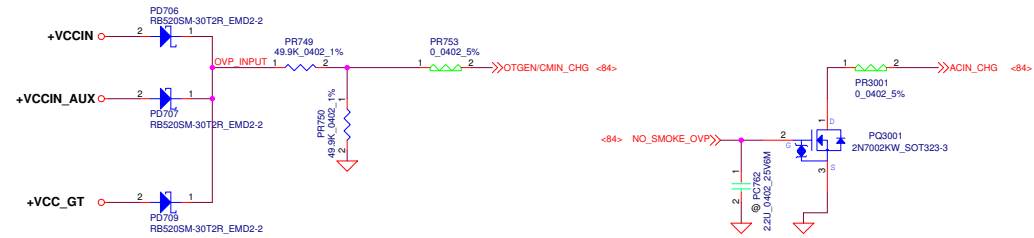
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IMVP VR OVP Circuit




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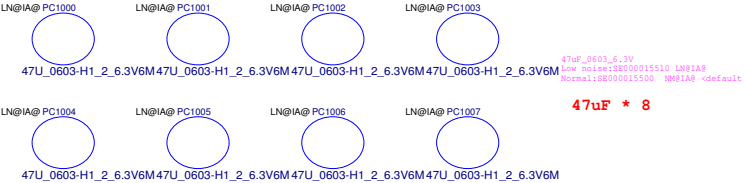
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+VCCIN Output Low noise MLCC



+VCCIN input Low noise MLCC

2nd Source control

4.7U_0603_25VAM-D Low noise:8E0000015501 LN@IA@ 4.7U_0603_25VAM-D


AOZ23645 & AOZ23655



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Version Change List (P. I. R. List)					
Item	Page#	Date	Issue Description	Solution Description	Rev.
1		2021.07.26	Customer request	1.Update DDR5 5V Enable circuit. 2.Change 5V solution to SYV136A 3.Add PD201and in parallel with PR201 to connect PU200 enable pin and SIO_SLP_S4#	X01
2		2021.08.03	Vender fine tune value	1.Change PC505 to S CER CAP 12P 50V J NPO 0402(SE071120J80) from S CER CAP 0.01UF 25V K X7R 0402(SE068103K80)	X01
3		2021.08.05	Vender fine tune value	1.Change PCX220 to 220P_0402_50V7K(SE074221K80) from 390P_0402_50V7K(SE074391K80) 2.Change PRZ09,PRZ32 to 4.02K_0402_1%(SD034402180) frim 2.1K_0402_1%(SD034210180) 3.Change PRZ16 to 169K_0402_1%(SD034169380) from 165K_0402_1%(SD034165380) 4.Change PRZ103 to 32.4K_0402_1%(SD034324280) from 34K_0402_1%(SD034340280)	X01
4		2021.08.18	EMI request.	1.Pop PR112 2.Pop PCX125	X01
5		2021.08.18	EE request for DDR5 secqence	1.Change PR245 Pin1 net to SIO_SLP_SUS# from 3V5V_EN	X01
6		2021.08.23	PUV1 VCC33 power rail change to +3.3V_ALW from +3.3V_RUN can fix cold boot NVVDD_PG glitch	1.Add PRV37 4.7_0402_5%(SD028470B80) connect to +3.3V_ALW and NVVDD_VCC33 2.Depop PRV2	X01
7		2021.08.25	RF request	1.Reserve PC1057,PC1058PC1059,PC1063,PC1064 220P_0402_50V7K(SE074221K80) 2.Reserve PC1060,PC1061,PC1062,PC1065,PC1066 100P_0402_50V8J(SE071101J80)	X01
8		2021.08.27	Change for THM air flow	1.Add PCH52,PCH53 and Pop 2.De-pop PCH12,PCH19	X01
9		2021.09.01	Vender fine tune value for Rev.5	1.Change PR541 to 11K_0402_1%(SD034110280) from 14.3K_0402_1%(SD00000QM80)	X01
10		2021.09.08	For Intel change GT core lccMAX 626774_ADL_MOW_WW36_2021	1.Change PRZ33 to 53.6K_0402_1%(SD034536280) from 49.9K_0402_1%(SD034499280) 2.Change PRZ103 to 33.2K_0402_1%(SD034332280) from 32.4K_0402_1%(SD034324280) 3.Change PRZ107 to 24.3K_0402_1%(SD00000AT80) from 20.5K_0402_1%(SD034205280)	X01
<div> <div>  <div> <div>DELL CONFIDENTIAL/PROPRIETARY</div> <div>Compal Electronics, Inc.</div> <div>PWR P.I.R</div> <div>LA-L871P</div> <div> <div> <div>Size</div> <div>Document Number</div> <div>Date: Tuesday, January 18, 2022</div> </div> <div> <div>Rev</div> <div>1.0</div> <div>Sheet 119 of 128</div> </div> </div> </div> </div> <div> PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC.. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL.. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT. </div> </div>					

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線寬線距<3.5mil, or 線距>12mil 不建議使用

40 ± 4 ohm single-end	46 ± 4.6 ohm single-end	48 ± 4.8 ohm single-end	60 ± 6 ohm single-end	62 ± 6.2 ohm single-end	80 ± 8 ohm Diff.	83 ± 8.3 ohm Diff.	86 ± 8.6 ohm Diff.	88 ± 8.8 ohm Diff.	86 ± 8.6 ohm Diff.	90 ± 9 ohm Diff.	Ref	100 ± 10 ohm Diff.	R
trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)		trace Width (±12%)	
			13.2						10.4.5	8.5/4.5	L3	12/5	no R
			49.49						84.57	90.14		100.75	
												11/6.5	no R
												99.63	
5	4.8	4.3	3.8	3.5	4/3.5	3.7/3.5	3.5/3.5	3.5/4.2		4.0/6.0	L4/L6	10/6.5	no R
39.87	44.80	47.45	50.03	51.88	80.1	82.59	84.91	87.85		90.04		99.46	
6	4.8	4.3	3.8	3.5	4/3.5	3.7/3.5	3.5/3.5	3.5/4.2		4.0/6.0	L5/L7	10/6.5	no R
			13.2						10.4.5	8.5/4.5	L6	12/5	no R
			49.49						84.57	90.14		100.75	

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LAN Clarkvillie

NVPRO@UL1

WG1219V SLKJ4 A0 QFN
SA00009345L

Precision

14P@ RE25

1K_0402_5%
SD028100180

ROM_Chip(NVPRO@)

NVPRO@ UC2

XM25RH256CXIQT10S
SA0000E1500

RC142

NVPRO@

SD000000TO00

49.9_0201_1%

RC144

NVPRO@

SD000000TO00

49.9_0201_1%

EC Chip

5200C@ UE1

MEC5200M-D0-I/LJ WFBGA KB CTRL REVC
SA0000DIF20

TBT RETIMER PS8830

PS8830@UT1

PS8830

NEW00000000

PS8830@RT148

PS8830

NEW00000000

PS8830@UT2

PS8830

NEW00000000

PS8830@RT213

PS8830

NEW00000000

4.99K_0402_1% 4.99K_0402_1%
SD034499180 SD034499180

5107 EC Chip

5107ES@ UE1

MEC5107KD4LJTR_WFBGA176P-NH
SA0000CG730

5107NES@ UE1

MEC5107KD4LJTR_WFBGA176P-NH
SA0000CG740

TPM_Chip

NU@ UZ4

NPCT750JADYX
SA0000AQ2C0

AHE0@ UZ4

ST33HTPH2X32AHE0
SA0000CY060

X76_ROM_Chip(VPRO@)

WBVPROX76@ ZZZ

ALT. GROUP PARTS WINDB VPRO BIOS HDB45
X7692731L53

GDVPROX76@ ZZZ

ALT. GROUP PARTS GD VPRO BIOS HDB45
X7692731L54

XMCVPROX76@ ZZZ

ALT. GROUP PARTS XMC VPRO BIOS HDB45
X7692731L55

CPU

QXZT@ UC1

FJ8071504698606
SA0000EL90L

QYZM@ UC1

FJ8071504786704 QYZM
SA0000F4V0L

QYYD@ UC1

FJ8071504787906 QYYD
SA0000F4X0L

QYYC@ UC1

FJ8071504786903 QYYC
SA0000F4W0L

SRLD8@ UC1

FJ8071504786907 SRLD8
SA0000FBY1L

QYLV@ UC1

FJ8071504698610
SA0000EVK0L

QYY9@ UC1

FJ8071504786603 QYY9
SA0000F4A0L

Q07L@ UC1

FJ8071504786505
SA0000F9B0L

SRLD9@ UC1

FJ8071504787907 SRLD9
SA0000F9F2L

QYY8@ UC1

FJ8071504786504 QYY8
SA0000F4U0L

Q07P@ UC1

FJ8071504786907
SA0000FBY2L

Q07N@ UC1

FJ8071504786705
SA0000F9C0L

SRLD7@ UC1

FJ8071504786708 SRLD7
SA0000FBW1L

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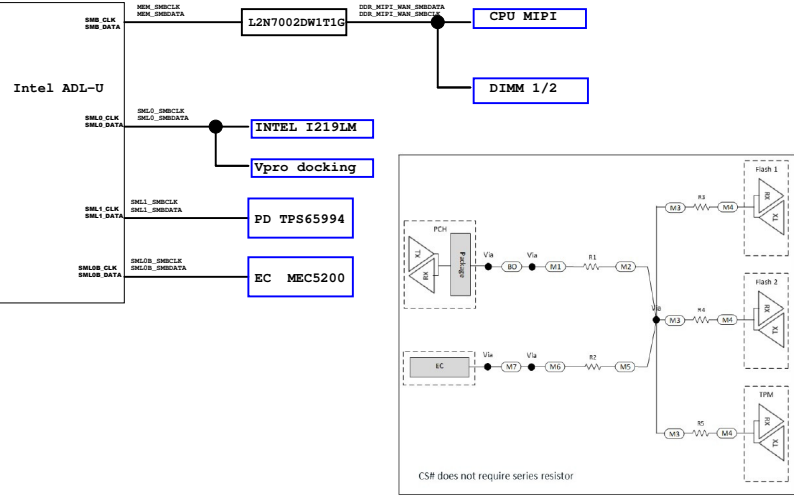
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SMBUS Block Diagram

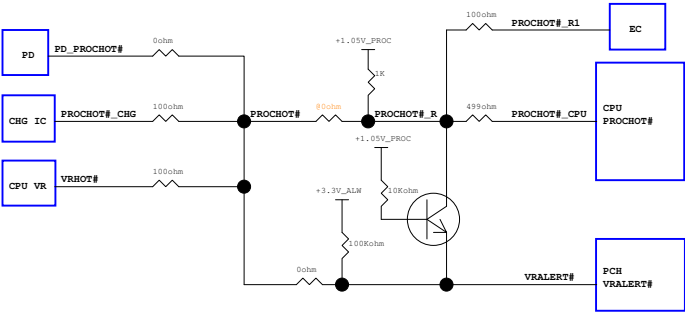


IO(L510)/Interfaces/SPI0 Flash/2-Load Branch Topology (Device Down) with EC Wire-OR Flash Sharing and TPV Segments					
Segment	Time Type	Reference	Via Count	Max Length, Segment (mm)	Max Length, Total (mm)
BO/M7	MISL	VSS	1	12.7	
M1/M6	MISL/DSL	VSS	1	76.2	
M2/M5	MS	VSS	0	25.4	165.1
M3	MS	VSS	0	25.4	
M4	MS	VSS	0	25.4	

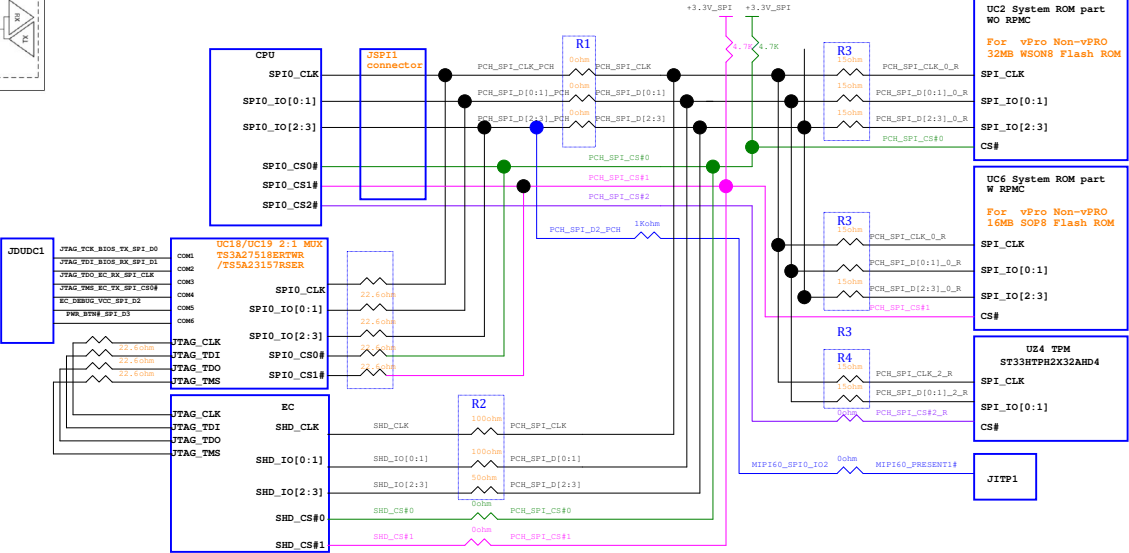
Note	Detail
Number of vias allowed	5
Reference plane	Continuous ground only
Max Frequency	50MHz
EC and PCH branch requirement	Delta between M1+M2 and M5+M6 shall not exceed 25.4mm (1inch)
M1/M6	It can be extended up to 76.2mm for 1.8V ONLY
R1	0Ω placeholder for 1.8V and 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO_2 and SPI0_IO_3
R2	[1] 15Ω for 1.8V and 100Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI. [2] 50Ω for 1.8V and 50Ω for 3.3V. To be placed on SPI0_IO_2 and SPI0_IO_3. If TPM use this signal, R2 value shall follow MISO and MOSI recommendation.
R3	15Ω for 1.8V and 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO_2 and SPI0_IO_3
R4	15Ω for 1.8V and 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO_2 and SPI0_IO_3
R5	15Ω for 1.8V and 3.3V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI. If TPM use SPI0_IO_2 and SPI0_IO_3, R5 value shall follow MISO and MOSI recommendation.
Minimum length	[1] M1, M3, M4 and M6: 12.7mm [2] R2 and M5: 2.54mm
M3 + M4	SPI branches of segment M3+M4 need to have length matching of 2.54mm
Device AC Timing Characteristics	Data Input Setup time < 2ns for 1.8V and 3.3V Data Input Hold time < 3ns for 1.8V and 3.3V 1.5ns < Clock to Data output valid time < 7.5ns for 1.8V 1.5ns < Clock to Data output valid time < 7ns for 3.3V
Length matching between CLK and DATA/CS# signals	12.7mm
Trace spacing between DATA and DATA signals	0.250mm
Trace spacing between CLK and DATA/Other signals	0.375mm
Signal Name/Unit	SPI0_CLK, SPI0_MOSI_IO_0, SPI0_MISO_IO_1, SPI0_IO_3, SPI0_IO_2, SPI0_CS0[1]#, SPI0_CS2#

6-Ch 1:2 MUX	JDUC1 ST33HTPH2X32AH4 SPI_CLK SPI_IO[0:1] CS#
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PROCHOT# Topology

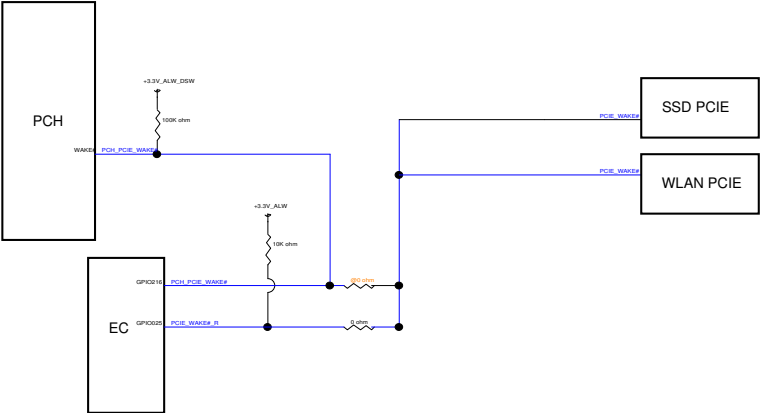


EC G3 SPI Flash Sharing with Wire-OR Non-Vpro / Vpro Topology

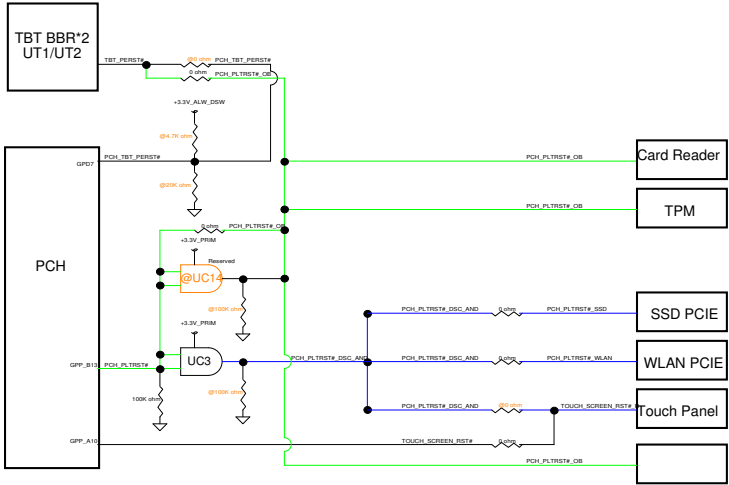


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PCH_PCIE_WAKE# Topology



PCH_PLTRST# Topology



Reserved Camera Truth Table for ALS/EMZA COS

Camera Truth table	Mc Only	from RGB Camera	from IR Camera	from EMZA Camera	from EMZA Camera w/o ALS	from EMZA Camera w 2nd ALS	from P-sen Camera	from P-sen Camera w/o ALS	from P-sen Camera w 2nd ALS
CAM_M0C_CBL_DET#(GPP_F14) (module det)	L	L	L	L	L	L	L	L	L
IR_CAM_DET#(GPP_A15) (cable det)	H	H	L	L	L	L	H	H	H
EMZA_DET#_IP8 (GPP_A16) (cable det/TBD)	H	H	H	L	H	L	L	H	L
GPP_D15(GPP_D15) (TBD)	H	H	H	L	L	L	H	L	L
Net name should be renaming like CAM_IDENTITY1~3	cable1	cable2	Cable3[no need to modify]	cable4-2:	cable4-3:	cable5-1:	cable5-2:	cable5-3:	
			JIR1.1 con to JIR1.10(GND)	JIR1.1 con to JIR1.10(GND)	JIR1.1 con to JIR1.10(GND)	JIR1.1 Floating	JIR1.1 Floating	JIR1.1 Floating	
			JIR1.13 con to GND(module)	JIR1.13 Floating	JIR1.13 con to GND(module)	JIR1.13 con to GND(module)	JIR1.13 Floating	JIR1.13 con to GND(module)	
			JIR1.4 Floating	JIR1.4 con to GND(module)	JIR1.4 con to GND(module)	JIR1.4 Floating	JIR1.4 con to GND(module)	JIR1.4 con to GND(module)	

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Other Topology-2

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